University of Anbar
College of Engineering
Dept. of Electrical Engineering

Lab. Name: EE Lab III (Electronic I)
Experiment no.: 1
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Experiment

CE Amplifier – Setting up the Rest Point

Object

- To Measure and verify DC operation point of the transistor amplifier (also called bios point or DC rest point).
- To investigate the meaning of Cut-off and Saturation.
- To investigate Influence of DC rest point over the maximum output signal swing.

Theory

The analysis or design of a transistor amplifier requires knowledge of both the DC and the AC response. The analysis or design of any amplifier therefore has two components: the DC portion and the AC portion. In fact, the improved output AC power level is the result of a transfer of energy from the applied DC supplies.

The term biasing refers to the application of DC voltages to establish a fixed level of current and voltage. For transistor amplifier, the resulting DC current and voltage establish an operating point on the characteristics that define the region that will be employed for the amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (Q-point. The biasing circuit should be designed to set the device operation at a Q-point within the active region. For the BJT to be biased in the active region, the following must be verified:

1. The base-emitter junction must be forward-biased, with a resulting forward-bias voltage of about 0.6 to 0.7V.
2. The base-collector junction must be reverse-biased, with the reverse-bias voltage being any value within the maximum limits of the device.

Biasing circuits:

- Fixed – bias circuit
- Emitter bias
- Voltage divider bias

- DC bias with voltage feedback
- Miscellaneous bias

In the fixed bias circuit, the bias current I_{CQ} and voltage V_{CEQ} are functions of the current gain β of the transistor. However, because B is temperature sensitive, especially for silicon transistors, this may result in change in bias current and voltage. Therefore, it would be desirable to develop a bias circuit that is independent of the transistor beta.

The voltage divider circuit shown in Figure below is such a circuit. Voltage-Divider

bias circuit is often used because the base current is made small compared to the currents through the two base (voltage-divider) resisters. Consequently, the base voltage and therefore the collector current are stabilized against changes in the transistor beta.

❖ Voltage Divider Bias

- This is the most widely used method to provide biasing and stabilization to a transistor
- In this form of biasing shown in Fig.1, R_1 and R_2 divide the supply voltage V_{CC} and voltage across R_2 provide fixed bias voltage V_B at the transistor base.
- Also, a resistance R_E is included in series with the emitter that provides the stabilization.

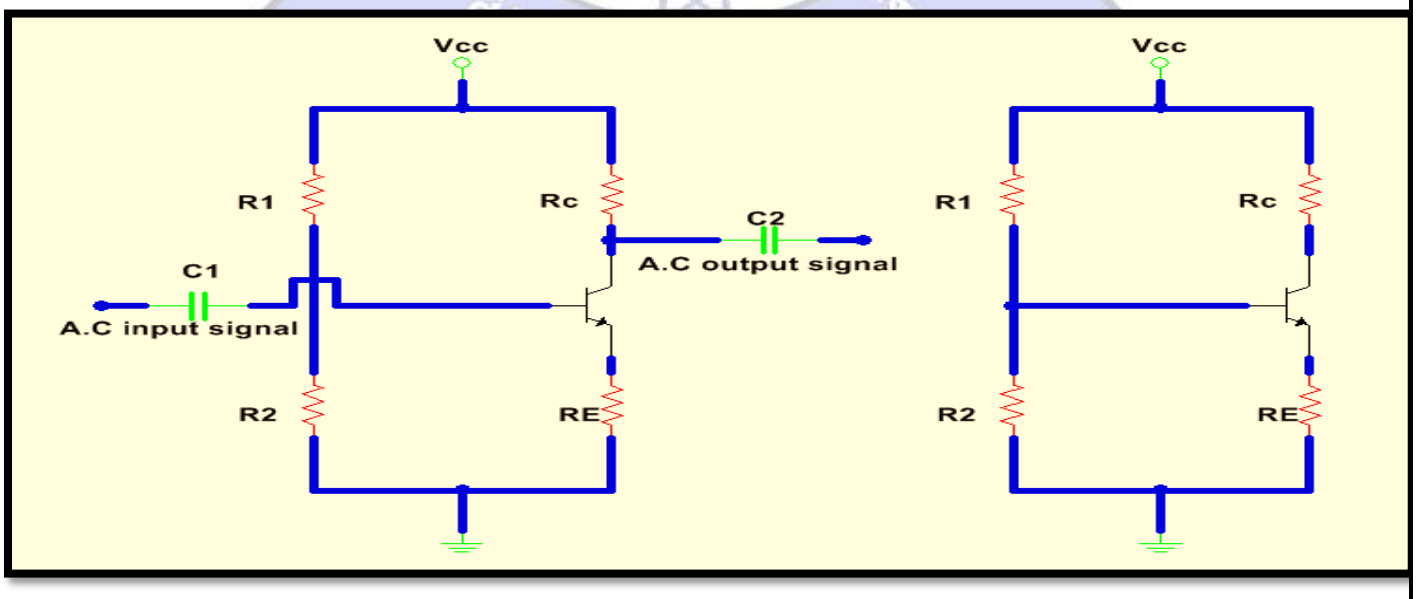

Fig.1

The approximate analysis of the voltage divider bias circuit can be established by neglecting the base current I_B when compared to the current flowing in resistor R2. This is justified by assuming that the input resistance seen from the base is much greater than R_2 ($R_1 = \beta R_E >> R_2$). Thus, the necessary condition for the approximate analysis of the circuit.

When: -

$V_B = Voltage\ across\ R_2$ (ignoring base current)

$$\boldsymbol{V_B = V_{CC}\frac{R_2}{(R_1 + R_2)}}$$

$$\beta R_E. \geq 10R_2$$

In this case, the bias voltage is given by:

$$\boldsymbol{V_B = V_{CC}\frac{R_2}{(R_1 + R_2)}}$$

The D.C Emitter voltage is given by:

$$V_E = V_B - V_{BE}$$

Quiescent DC collector current can be found from:

$$I_{CQ} \cong I_{EQ} = \frac{V_E}{R_E}$$

Collector voltage is found by:

$$V_C = V_{CC} - I_{CQ}.R_C$$

The quiescent DC collector-emitter voltage is calculated from:

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$

The collector saturation current in this case given by:

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C + R_E}$$

$V_{CE(sat)}$ is approximately equal to 0.2V for silicon transistor. The collector-emitter voltage at cut-off is: $\boxed{V_{CE(off)} = V_{CC}}$

Procedures

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal. The analysis or design of any electronic amplifier therefore has two components:

M100- Transistor Amplifiers- Components Lists	
R1	22K
R2	4K7
R3	39K
R4	470Ω
R5	3K3
R6	2K7
R7	10K
R8	1K5
R9	3K3
C1	100KpF=100nF
C2	1µF
C3	100KpF=100nF
C4	1µF
C5	100KpF=100nF
P1	Trimmer 47K
P2	Trimmer 4K7
Q1	BC337
Q2	BC337

Table 1

A) The dc portions.

Wire the board as shown in Fig.1, then precede as follows:

- Adjust P_1 around its position. See the consequent change in V_C. This happens since P_1 changes the base current of Q_1 and turn its emitter and collector currents ($\boldsymbol{I_E \sim I_C = h_{fe}.I_b}$).

  A charging collector current determines a charging voltage drop across the load resistor R_5.
- Move P_1 to its extreme positions, corresponding to saturation ($V_{CE} = 0$) and cut-off ($\boldsymbol{V_{CE} = V_{CC}}$).

  Start with cut-off:

  Measure V_{CE} and the voltage drop across R_5. This last figure should be very low, meaning that only a negligible current flow in the cut-off point on the graph of Fig.2, representing the transistor charstristics.

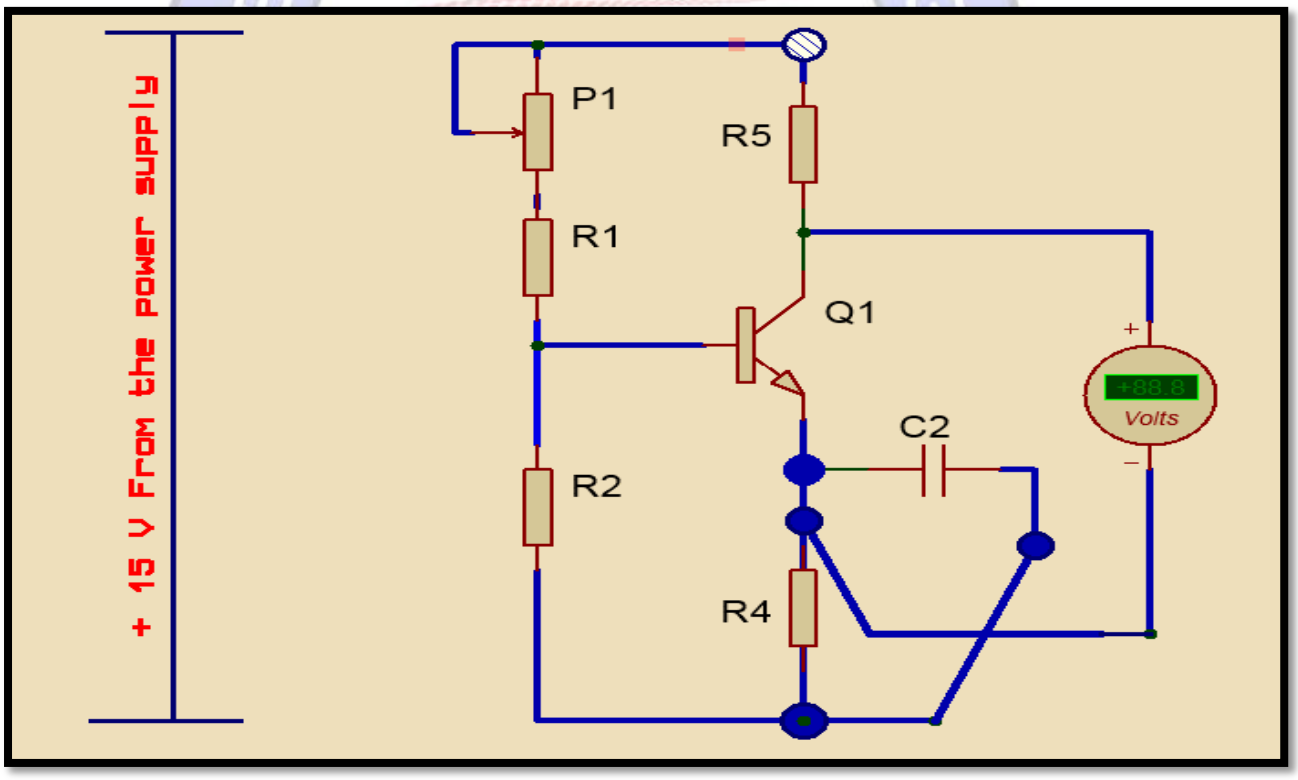

Fig.1: Setup to study the DC biasing of CE amplifier

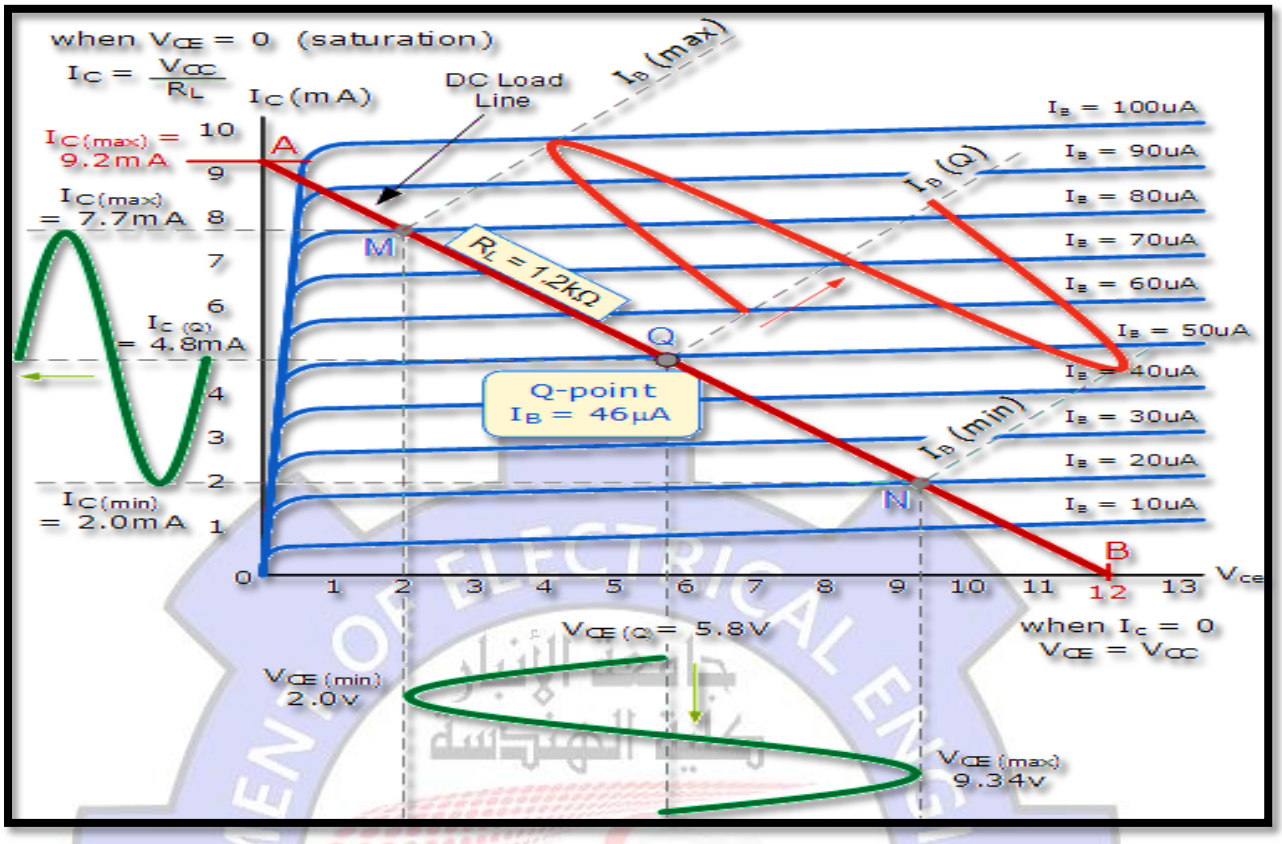

Fig.2: Drawing the load line for the transistor amplifier (an example)

- Move P_1 to achieve saturation.
  Measure V_{CE} , then drop across R_5 and from this calculate the saturation current.

  Mark this second point on the graph of Fig.2 (saturation point).
- Draw by a straight line the two points marked on Fig.2. this is the static load line for the transistor amplifier.
- Adjust P_1 to an intermediate position, so as to have a V_{CE} of approx. $^{15V}/_{2}$.

  Do not move P_1 for the rest of the exercise.

  Measure V_{CE} again and the voltage drop on R_5, calculate I_C. Plot this new point on the same graph of Fig.2. the point should lie on the line previously drawn.

- Measure the voltage across R_2 and across R_4. Check that the two differ by approx. 0.5 to 0.7. this is the drop across the directly biased B-E junction of the transistor.
- Change the wiring of the module Fig.3. by connecting a sine-wave generator, approx. 20mVapp, 10KHz at the base input, while monitoring the collector signal by the oscilloscope.

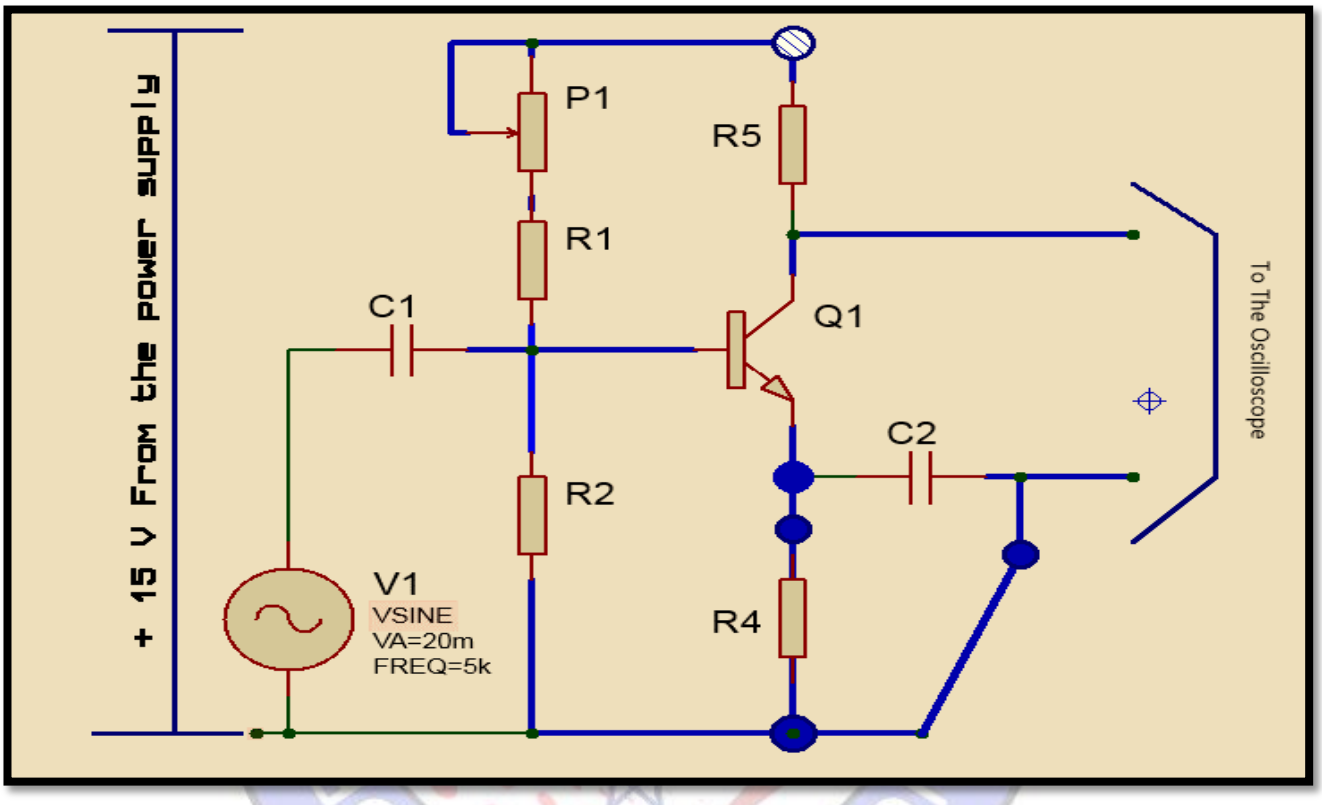

Fig.3: setup to study the output signal swing M100F3

B) The AC portions.

During the design stage, the choice of parameters for the required dc levels will affect the ac response. The most common circuit configuration for an NPN transistor is that of the Common Emitter Amplifier and that a family of curves known commonly as the Output Characteristics Curves, relates the Collector current (I_C), to the output or Collector voltage (V_{CE}), for different values of Base current (I_B). All types of transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value. Presetting the amplifier circuit to operate between these two maximum or peak values is achieved using a process known as Biasing. Biasing is very important in amplifier design as it establishes the correct operating point of the

transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal.

- Adjust the input amplitude to make the output signal appear as in Fig.4A or 4B, i.e. a sinewave dipped on top (cut-off) or bottom (saturation).

Fig.4A - DC Bias point too near to saturation

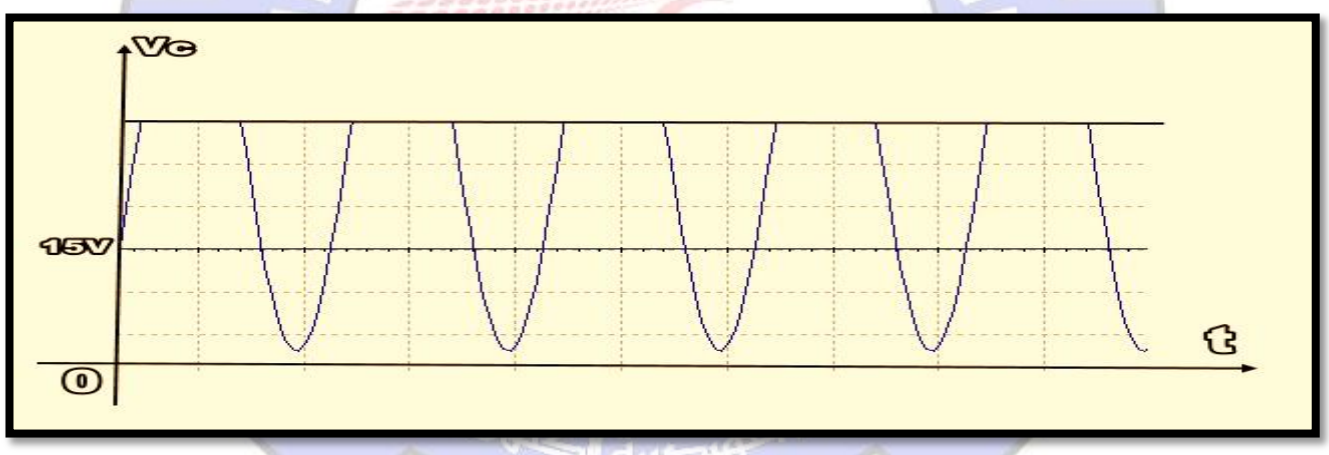

Fig.4B - DC Bias point too near to cut-off

- Adjust Pl and the input level to make the output signal appear as on undistorted sinewave of max. amplitude. Remove the generator and determine the new DC bias point Fig.2. This is the working point which allows the largest swing for the output signal.
  Explain this
- Measure the input and output signal amplitude with the oscilloscope. Calculate from these figures the amplifier Voltage Gain.

Results tables

A) The DC portions

V_{CE}(v)	V_{RC} (v)	IC (mA)	VR4 (v)	VR2 (v)	VBE (v)

B) The AC portions

V_{CE} (v)	V_{RC} (v)	IC (mA)	Vout (+peak)	Vout (-peak)

Discussion

1-What is the phase relationship between the input and output signals of The CE amplifier, explain taking the load line into account.

2-What is mean by saturation region, active region and cutoff region? Mark the regions on the output characteristics.

3-Sketch the DC load line for the voltage – Divider bias circuit and place the Q-point on it.

4-It is desirable to have the Q-point centered on the load line. Why؟

5-In common emitter amplifier (CE), why the capacitors C_1, C_2 and CE are used?

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Experiment

CE Amplifier – Measurement of input resistance and output resistance

Object

To be familiarized with the measurement of the input resistance and output resistance of a Bipolar Junction Transistor common emitter single-stage amplifier.

Theory

The figure below shows a common-emitter amplifier with voltage-divider bias and coupling capacitors C1 and C3 on the input and output and a bypass capacitor, C2, from emitter to ground. The input signal, Vin, is capacitively coupled to the base terminal, the output signal, Vout, is capacitively coupled from the collector to the load. The amplified output is 180° out of phase with the input. Because the ac signal is applied to the base terminal as the input and taken from the collector terminal as the output, the emitter is common to both the input and output signals. There is no signal at the emitter because the bypass capacitor effectively shorts the emitter to ground at the signal frequency. All amplifiers have a combination of both ac and dc operation, which must be considered, but keep in mind that the common-emitter designation refers to the ac operation.

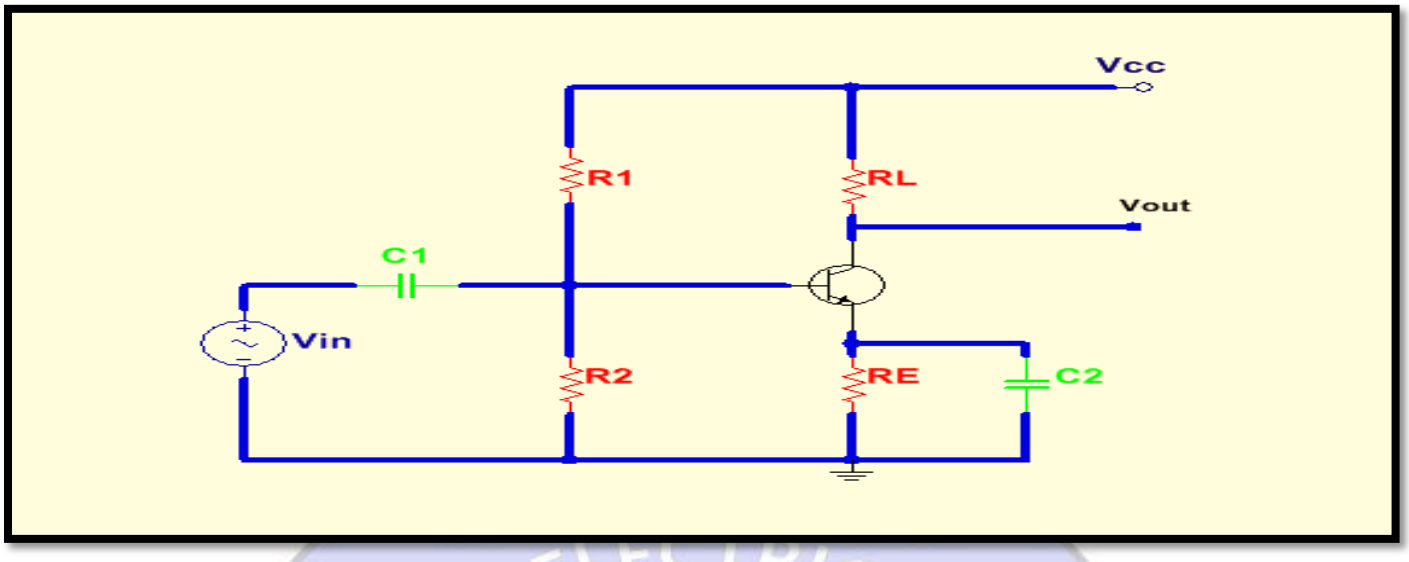

Fig 1: A common-emitter amplifier.

AC Analysis

To analyze the ac signal operation of an amplifier, an ac equivalent circuit is developed as follows:

1 .The capacitors C_1, C_2, and C_3 are replaced by effective shorts because their values are selected so that X_C is negligible at the signal frequency and can be considered to be 0 Ω.

2 .The dc source is replaced by ground.

A dc voltage source has an internal resistance of near 0Ω because it holds a constant voltage independent of the load (within limits); no ac voltage can be developed across it so it appears as an ac short. This is why a dc source is called an ac ground. The ac equivalent circuit for the common-emitter amplifier in Fig.1 is shown in Fig.2. Notice that both R_C and R_1 have one end connected to ac ground (red) because, in the actual circuit, they are connected to V_{CC} which is, in effect, ac ground.

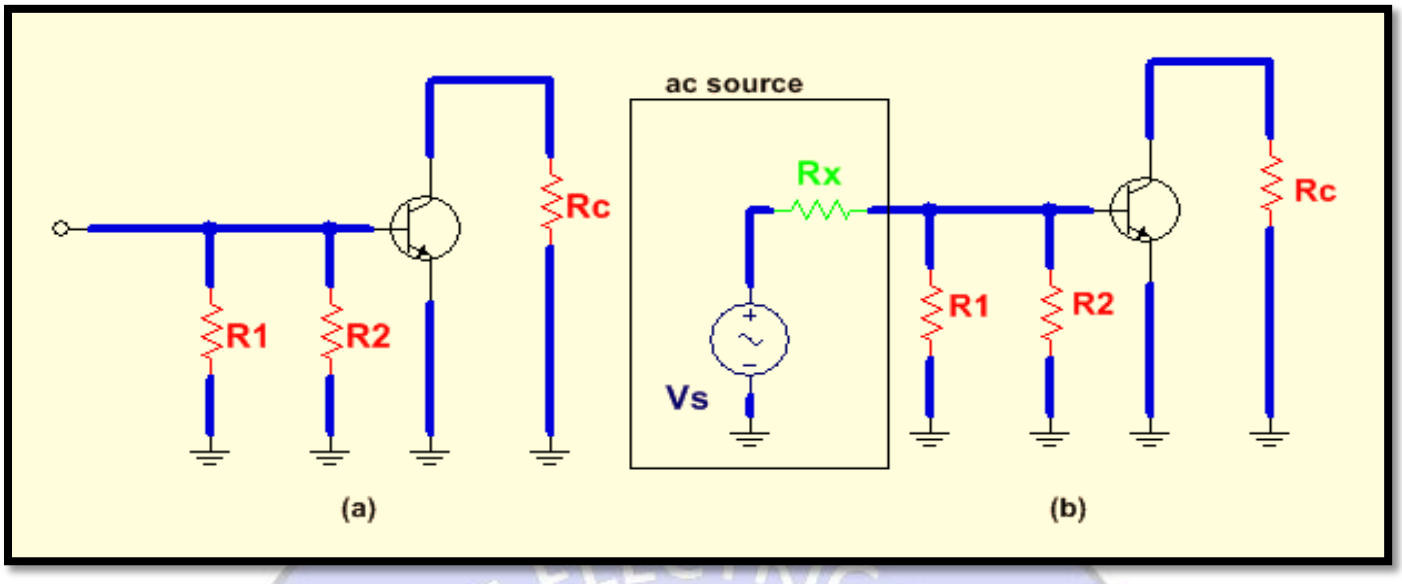

Fig.2: AC equivalent circuit for the amplifier in Fig.1

(a) without an input signal voltage. (b) with an input signal voltage.

In AC analysis, the ac ground and the actual ground are treated as the same point electrically. The amplifier in Fig.1 is called a common-emitter amplifier because the bypass capacitor C_2 keeps the emitter at ac ground. Ground is the common point in the circuit.

Signal (AC) Voltage at the Base An ac voltage source, Vs, is shown connected to the input in Fig.2(b). If the internal resistance of the ac source is 0Ω then all of the source voltage appears at the base terminal. If, however, the ac source has a nonzero internal resistance, then three factors must be taken into account in determining the actual signal voltage at the base. These are the source resistance (Rs), the bias resistance ($R_1 \| R_2$) and the ac input resistance at the base of the transistor (Rin(base)). This is illustrated in Fig.2(a) and is simplified by combining R_1, R_2, and Rin(base) in parallel to get the total input resistance, Rin(tot), which is the resistance "seen" by an ac source connected to the input, as shown in Fig.2(b). A high value of input resistance is desirable so that the amplifier will not excessively load the signal source. This is opposite to the requirement for a stable Q-point, which requires smaller resistors. The conflicting requirement for high input resistance and stable biasing is but one of the many trade-offs that must be considered when choosing components for a circuit. The total input resistance is expressed by the following formula:

$$R_{in(total)} = R_1 \| R_2 \| R_{in(base)}$$

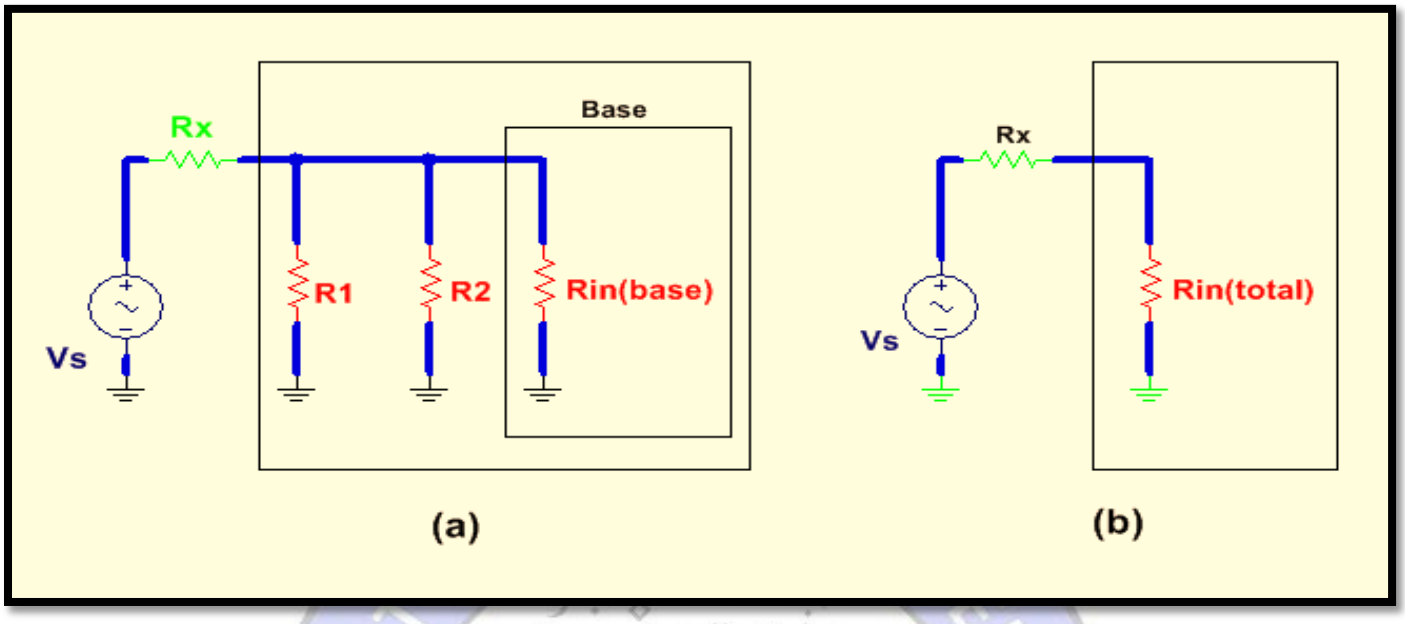

Fig.3: AC equivalent of the base circuit.

As you can see in the figure, the source voltage, Vs, is divided down by Rs (source resistance) and Rin(tot) so that the signal voltage at the base of the transistor is found by the voltage- divider formula as follows:

$$V_b = \left(\frac{R_{in(total)}}{R_s + R_{in(total)}}\right) V_s$$

If $R_s << R_{in(total)}$,then $V_b \cong V_s$,where V_b is the input voltage (V_{in}) to the amplifier

Input Resistance at the Base: To develop an expression for the ac input resistance looking in at the base, use the simplified r-parameter model of the transistor. Fig.4 shows the transistor model connected to the external collector resistor, RC. The input resistance looking in at the base is:

$$R_{in(base)} = \frac{V_{in}}{I_{in}} = \frac{V_b}{I_b}$$

The base voltage is

$$V_b = I_e \acute{I}_r$$

And since $I_e \cong I_{\acute{c}}$

$$I_b \cong \frac{I_e}{\beta_{ac}}$$

Substation for V_b and I_b

$$R_{in(base)}=\frac{V_b}{I_b}=\frac{I_e \acute{r}_e}{I_e/\beta_{ac}}$$

Cancelling $I_{\acute{e}}$

$$R_{in(base)}=\beta_{ac}\acute{r}_e$$

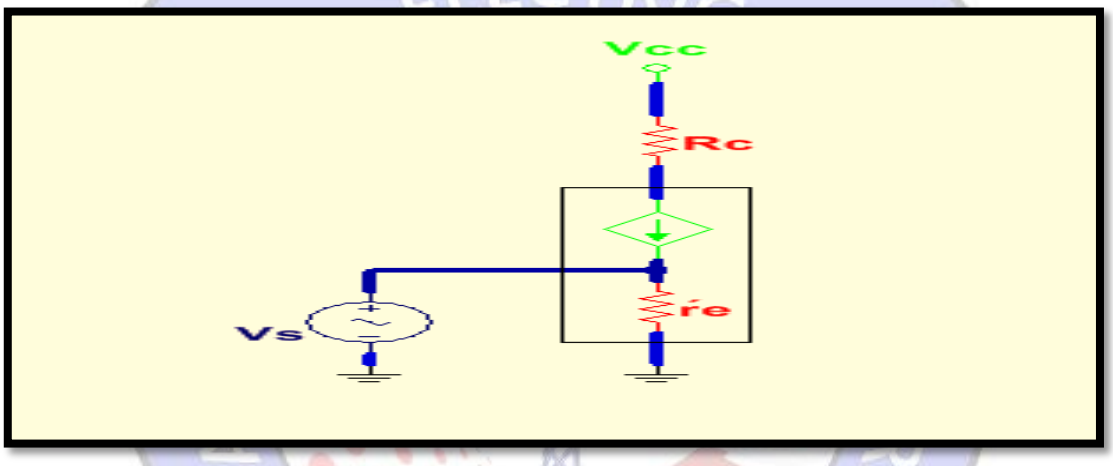

Fig.4: r-parameter transistor model (inside shaded block) connected to external circuit.

Output Resistance: The output resistance of the common-emitter amplifier is the resistance looking in at the collector and is approximately equal to the collector resistor.

$$R_{out} \cong R_c$$

Actually, $R_{out} \cong R_c \| \acute{r}_e$ but since the internal ac collector resistance of the transistor $\acute{r}_e$, is typically much larger than RC, the approximation is usually valid.

Procedures

M100- Transistor Amplifiers- Components Lists

R1	**22K**
R2	**4K7**
R3	**39K**
R4	**470Ω**
R5	**3K3**
R6	**2K7**
R7	**10K**
R8	**1K5**
R9	**3K3**
C1	**100KpF=100nF**
C2	**1µF**
C3	**100KpF=100nF**
C4	**1µF**
C5	**100KpF=100nF**
P1	**Trimmer 47K**
P2	**Trimmer 4K7**
Q1	**BC337**
Q2	**BC337**

Table 1

❖ CE Amplifier, Measurement of Input Resistance

The setup used for this exercise is shown in Fig.5.

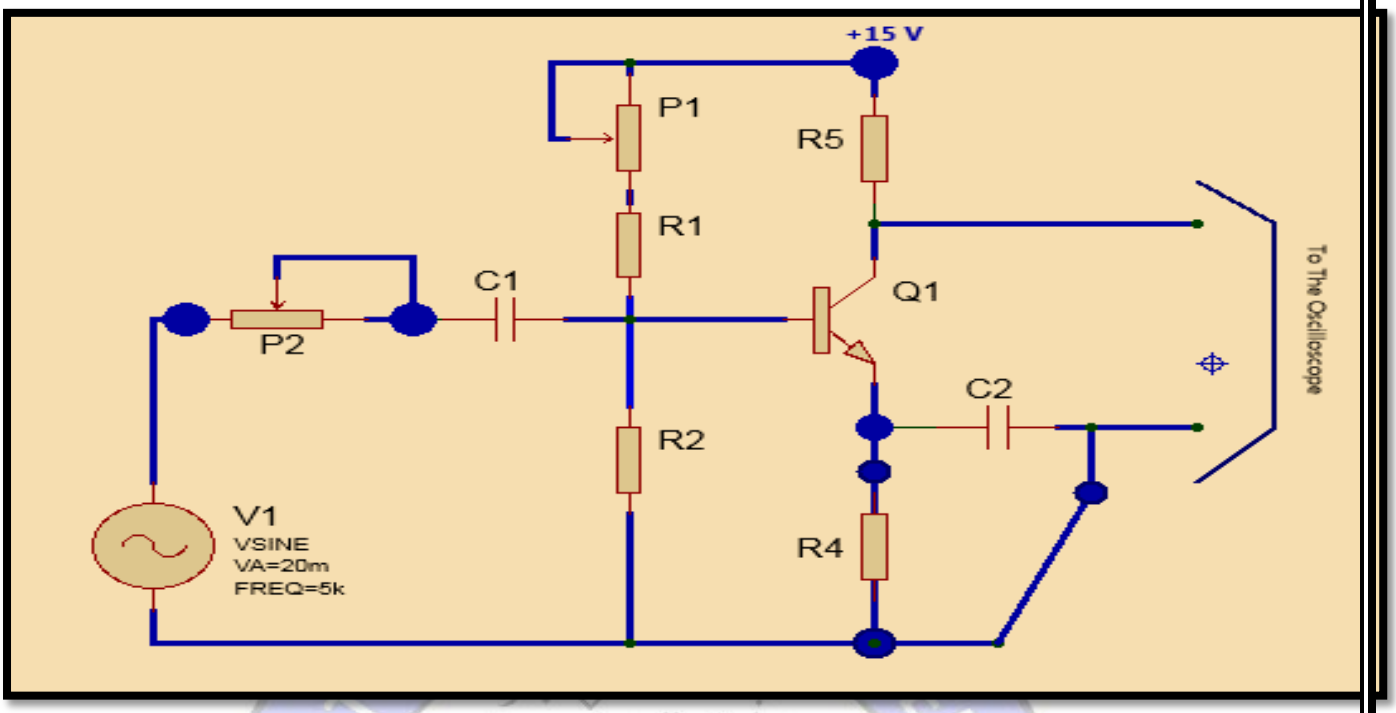

Fig.5 - Setup to determine the input R resistance of the CE AHP(M100IF5)

Basically, the difference with Fig.3 is that now we have a variable resistor placed in series with the generator feeding signal to the base input.

- The principle of the measurement is the following:

– The variable (P_2) resistor is initially set at 0 (short circuit). The generator is adjusted for l KHz sinewave and the amplitude is adjusted to have at the output an undistorted sinewave of, say, 5Vpp.

– P_2 is slowly raised from its initial null value, to a point where the amplifier output signa l is halved. This happens since the input signal is also halved. (see Fig .6), i.e. P_2 = Ri.

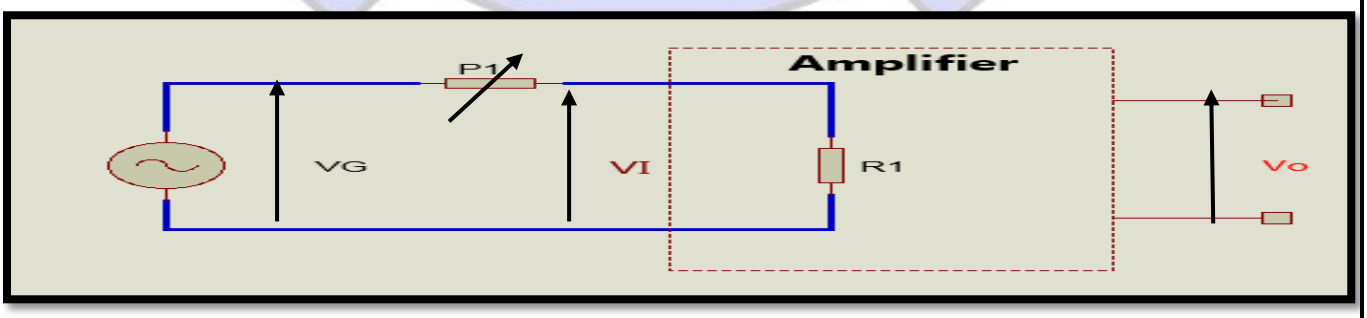

Fig.6 - Determination of the input resistance for the CE amplifier M1001F6

- The power supply is shut off, P_2 disconnected from the circuit and measured with on ohmmeter.
  This value equals the input impedance of the amplifier (refer to Fig.6)

While proceeding with the practical work, note the following:

- Choose for the frequency a high value (10KHz} in order to make C_1 and C_2 actually appear as short circuits to the AC signal.
- The gain of the amplifier is high, so the generator must be adjusted to deliver a low signal (10 to 50mVpp ore expected to be sufficient).

❖ CE Amplifier - Measurement of Output Resistance

The principle of this measurement is similar to that of the preceding case. Refer to Fig. 7, showing the setup, and to Fig.8 showing the equivalent schematic.

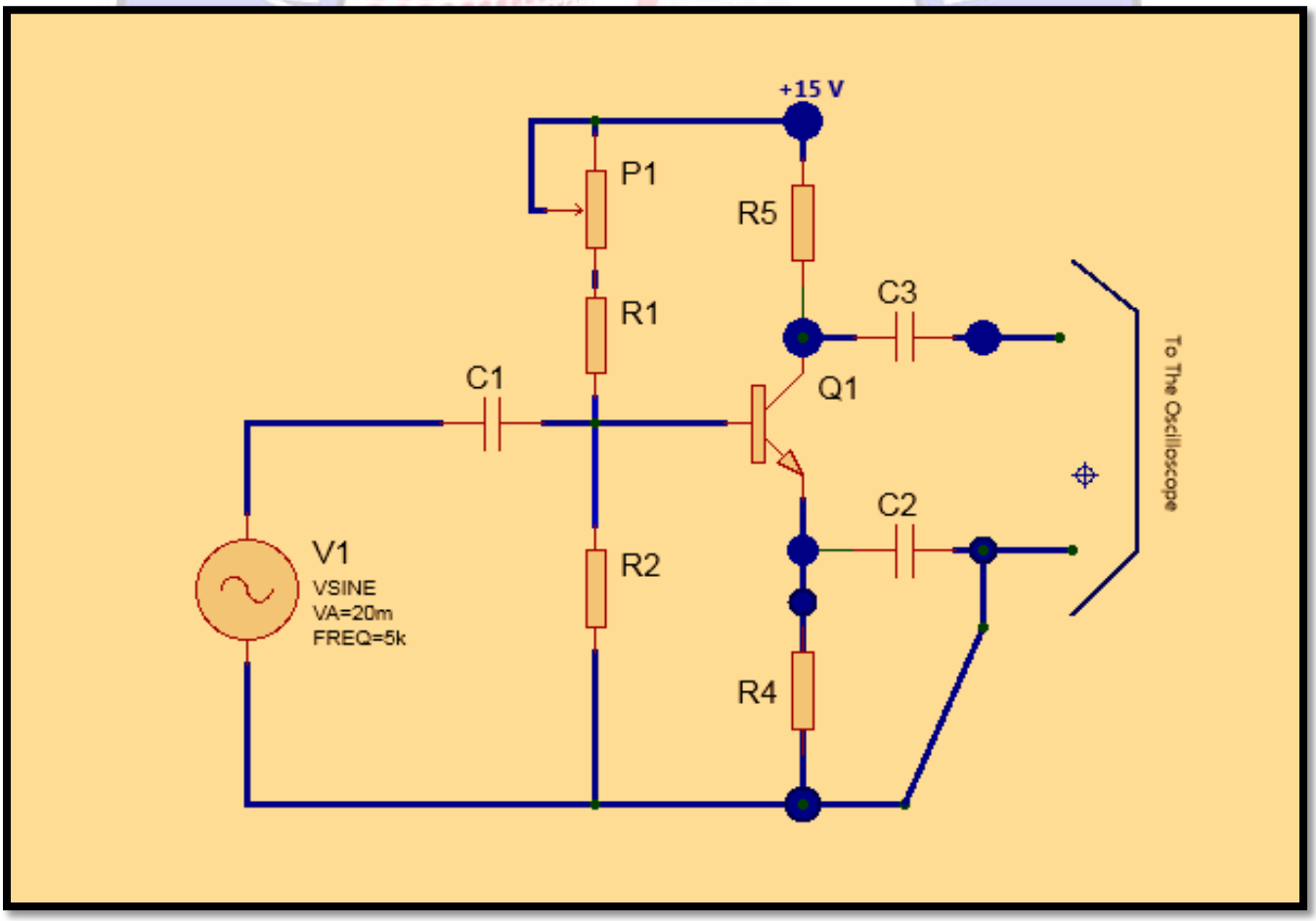

Fig.7 – Measurement of the output resistance M100F7

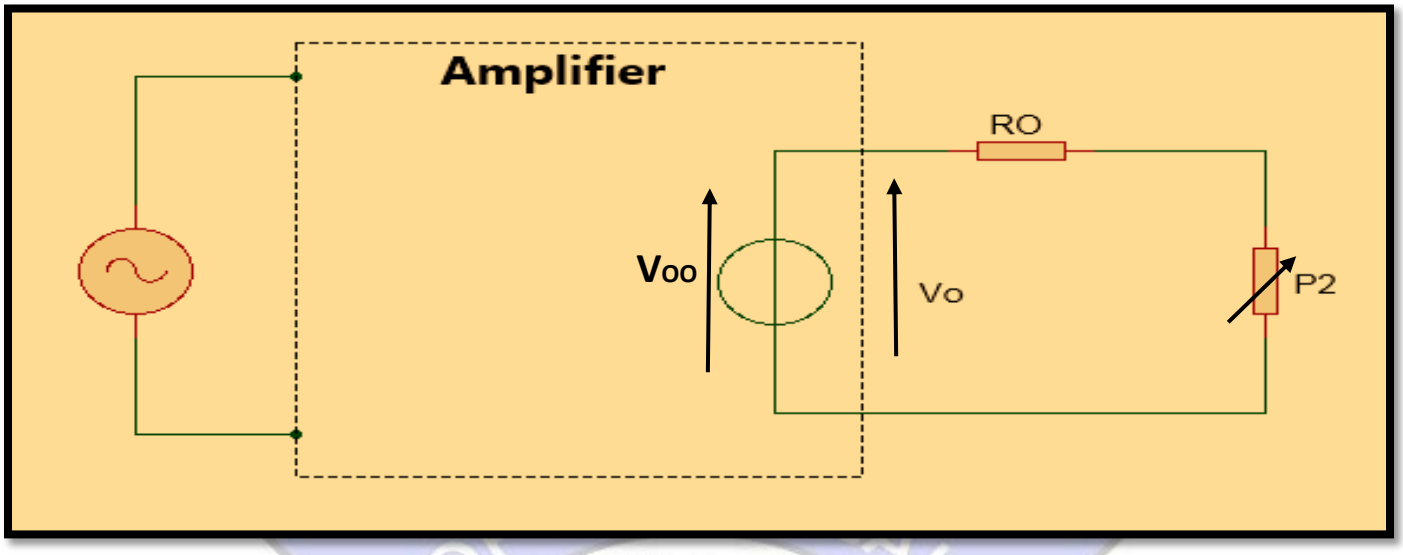

Fig.8 -The principle of the measurement, when $V_o = {}^1/_2\, V_{oo}$,then $P_2 = R_o$

- A 1OKHz sinewave is used as on input signal. Its amplitude is adjusted to convenient value to have an output of, for instance, 5Vpp. This should rein an input signal of 15 to 40mVpp.
- Trimmer P_2 is then connected as a load, DC decoupled by means of C_3. P_2 is adjusted to the point where the amplitude ·of the signal halves (with changing the level of the input signal).
  In these conditions P_2 hos a resistance equaling the output resistance of amplifier.

  Disconnect P_2 and measure it with an ohmmeter.

Results

Find input resistance and output resistance according to the previous mentioned procedures:

Discussion

Theoretically, find the values of input resistance and output resistance of common emitter transistor according to the setup that you have used during the procedures' steps. Compare between theoretical and practical results.

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Experiment

Amplifier Frequency Response

Object

The purpose of this experiment is to evaluate the frequency response of a common emitter amplifier.

Theory

All amplifiers have a finite bandwidth. The low cutoff frequency can in some cases extend down to DC and is a parameter under direct control of the designer. The ultimate high frequency limit is determined by the physical characteristics of the components and the construction of the circuit.

A typical BJT common emitter amplifier is shown in Fig.1. The input signal source and load resistor are capacitively coupled to the amplifier via capacitors C_{C1} *and* C_{C2} respectively. The coupling capacitors C_{C1} *and* C_{C2}, emitter bypass capacitor C_E, and internal transistor capacitances shape the frequency response of the amplifier.

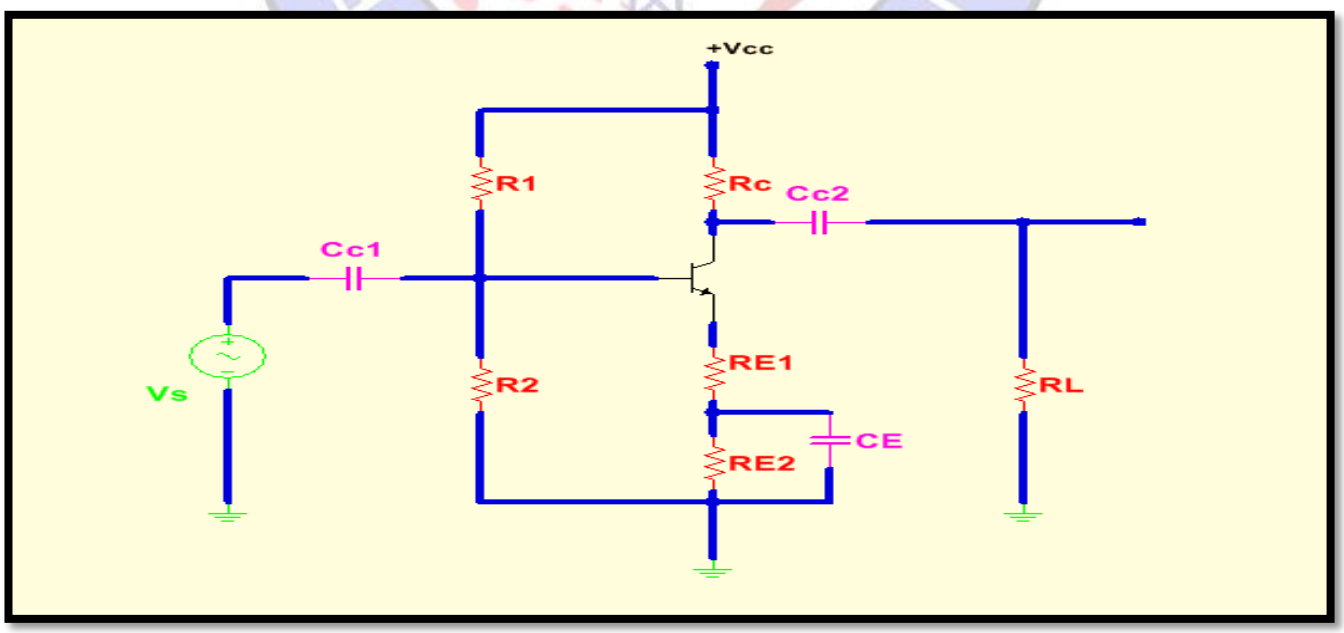


Fig.1: Typical Common Emitter Amplifier

A typical amplifier frequency response curve is shown in Fig.2. This curve presents the magnitude of the voltage gain versus frequency.

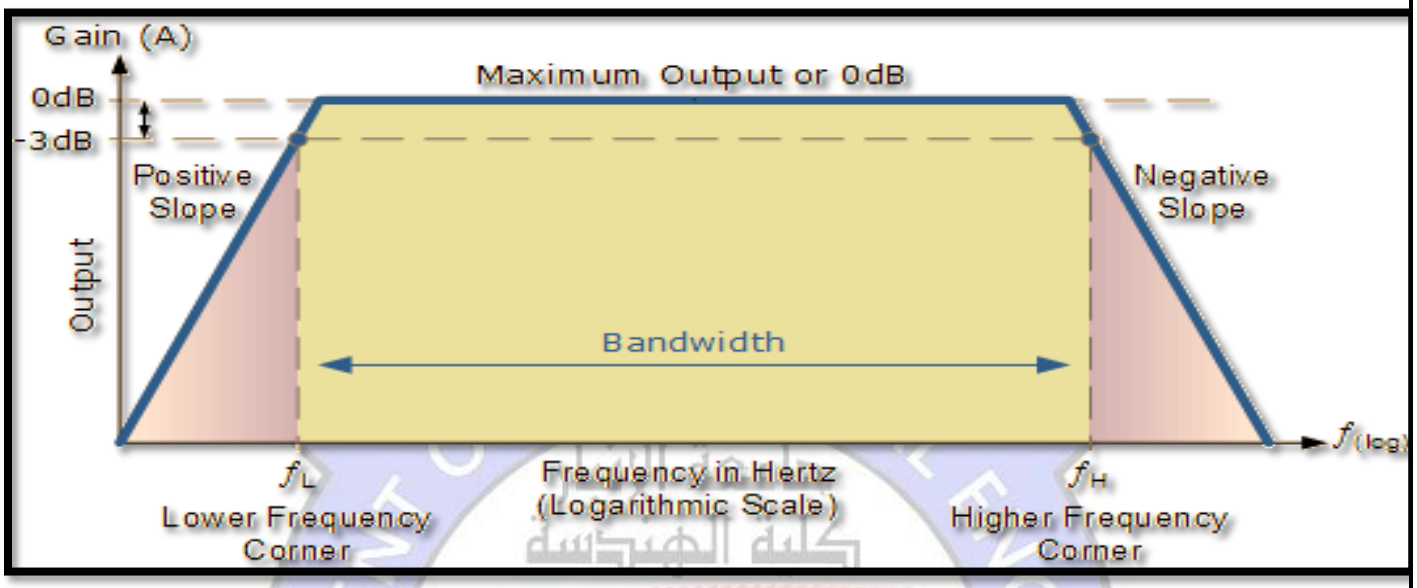


Fig.2: Typical Amplifier Frequency Response

The voltage gain in decibels is calculated as:

$$A_v = (dB) = 20Log(|A_v|)$$

In Fig.2, A_{vm} represents the mid-band (or mid range) gain of the amplifier. For the circuit of Fig.1, it is given by:

$$A_v = -\frac{(R_C \| R_L)}{r_e + R_{E1}}$$

At the lower cut-off frequency f_L and upper cut-off frequency f_H, the voltage gain of the amplifier drops to 0.707 of its mid-band values (or -3dB below the maximum value). The frequency f_L is dependent on the coupling and bypass capacitors, while the frequency $f_H$is determined by the transistor internal capacitances (mainly C_{bc} and C_{be}). The bandwidth of the amplifier is the difference between $f_H$and f_L:

$$BW = f_H - f_L$$

As the signal frequency drops below mid-band, the impedances of the coupling and bypass capacitors will increase, resulting in a reduction of the voltage gain. In other words, the low frequency response of the amplifier is determined by the capacitors C_{C1} , C_{C2} and C_E. Each one of the three capacitors make a contribution to the overall frequency response of the amplifier. Each capacitor behaves like a capacitor in a high pass filter. Therefore, each one will contribute with a cut-off frequency of its own.

The cut-off frequency due to the input coupling capacitor C_{C1} is f_{L1}, and is calculated from the following equation when ignoring the source resistance R_s:

$$f_{L1} = \frac{1}{2\pi . Z_{in} . C_{c1}}$$

Where Z_{in} is the input impedance of the amplifier and is given by:

$$Z_{in} = R_1 \| R_2 \| (\beta(r_e + R_{E1}))$$

The cut-off frequency due to the output coupling capacitor C_{c2} is f_{L2}, and is given by:

$$f_{L2} = \frac{1}{2\pi(R_C + R_L) . C_{c2}}$$

Finally, the cut-off frequency due to the emitter bypass capacitor $C_E$is f_{L3}, and is given by:

$$f_{L3} = \frac{1}{2\pi . Z_e . C_E}$$

Where $Z_e$is the effective emitter impedance seen from the terminals of capacitor C_E, and is given by:

- the source resistance Rs is so small to be ignored

$$Z_e = (r_e + R_{E1}) \| R_{E2}$$

Among the three corner frequencies, f_{L3} will usually have the largest value.

The low cut-off frequency of the amplifier can be approximated as the largest value of the three individual lower corner frequencies:

$$f_L = \max(f_{L1}, f_{L2}, f_{L3})$$

The high frequency response of the amplifier is determined by the internal parasitic capacitances of the transistor. These capacitances, C_{be} and C_{bc}, are proportional to the physical area of the junctions and inversely proportional to the width of the depletion region. This means that the capacitance is a function of bias conditions. A forward biased junction has relatively high capacitance (tens to over one hundred pico-farads) because the width of the depletion region is narrow. A reverse biased junction has relatively low capacitance (typically less than ten pico-farads) because the width of the depletion region is wide.

Two corner frequencies are existed due to the total transistor parasitic capacitances at input (base) and output (collector). The first corner frequency fH1 is inversely proportional to C_{be}+ C_M, where C_M is known as the Miller capacitance and is given by:

$$C_M = C_{be}.(1 + |A_{vm}|)$$

The second corner frequency f_{H2}, on the other hand, is inversely proportional to C_{bc}. The corner frequencies f_{H1} and f_{H2}can be determined from the high-frequency equivalent circuit of the amplifier.

The high cut-off frequency of the amplifier can be approximated as the lowest value of the two individual upper corner frequencies

$$f_H = \min(f_{H1}, f_{H2})$$

The frequency at which the amplifier's gain drops to 1 (or 0 dB) is called the unity-gain frequency and is denoted by f_T. The significance of f_T is that it always equals the product of the mid-band gain times the bandwidth of the amplifier.

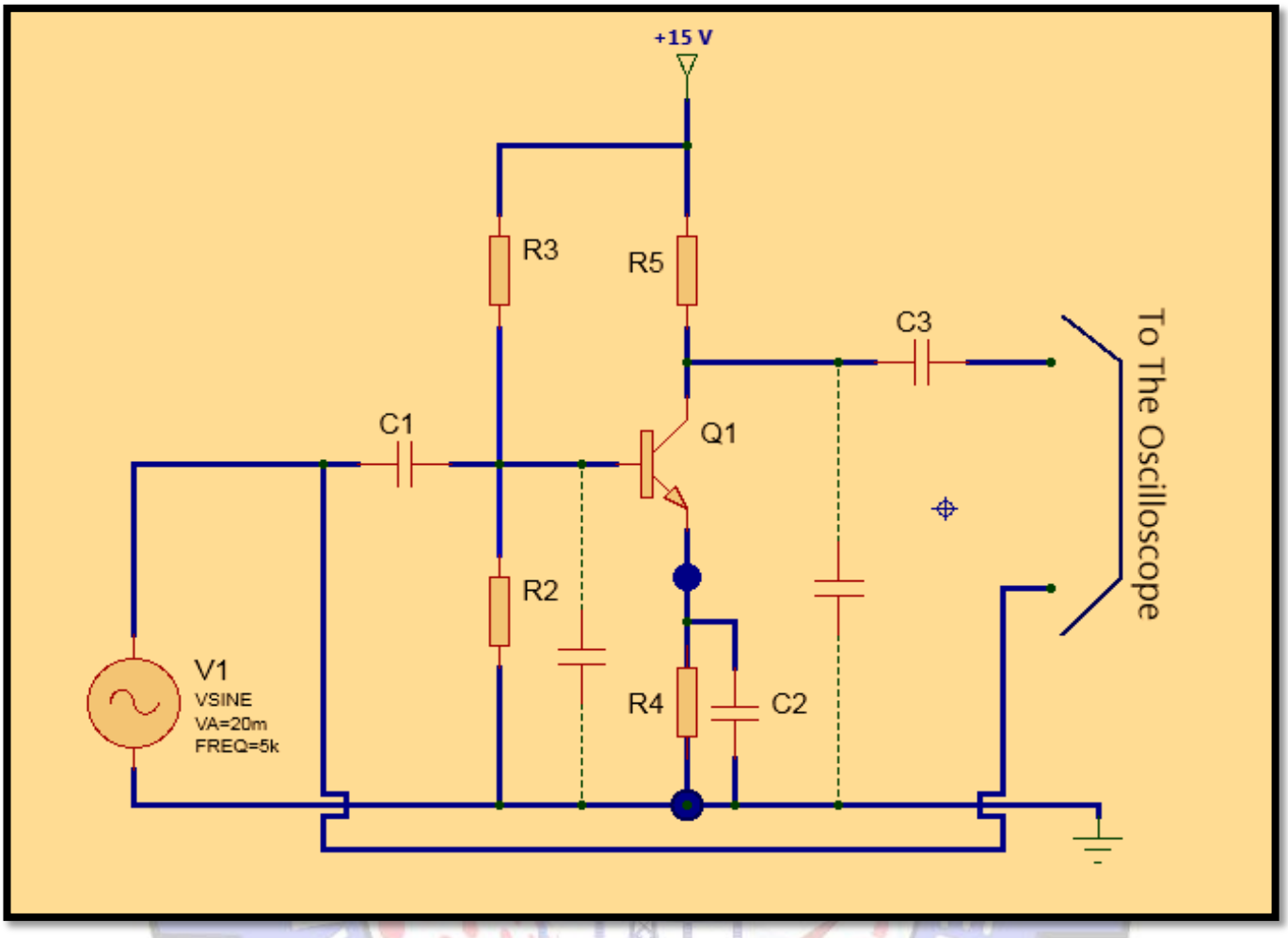
$$f_T = A_{vm}.BW$$

Procedures

1. Build the circuit shown in Fig.7 using the following components listed in the table below

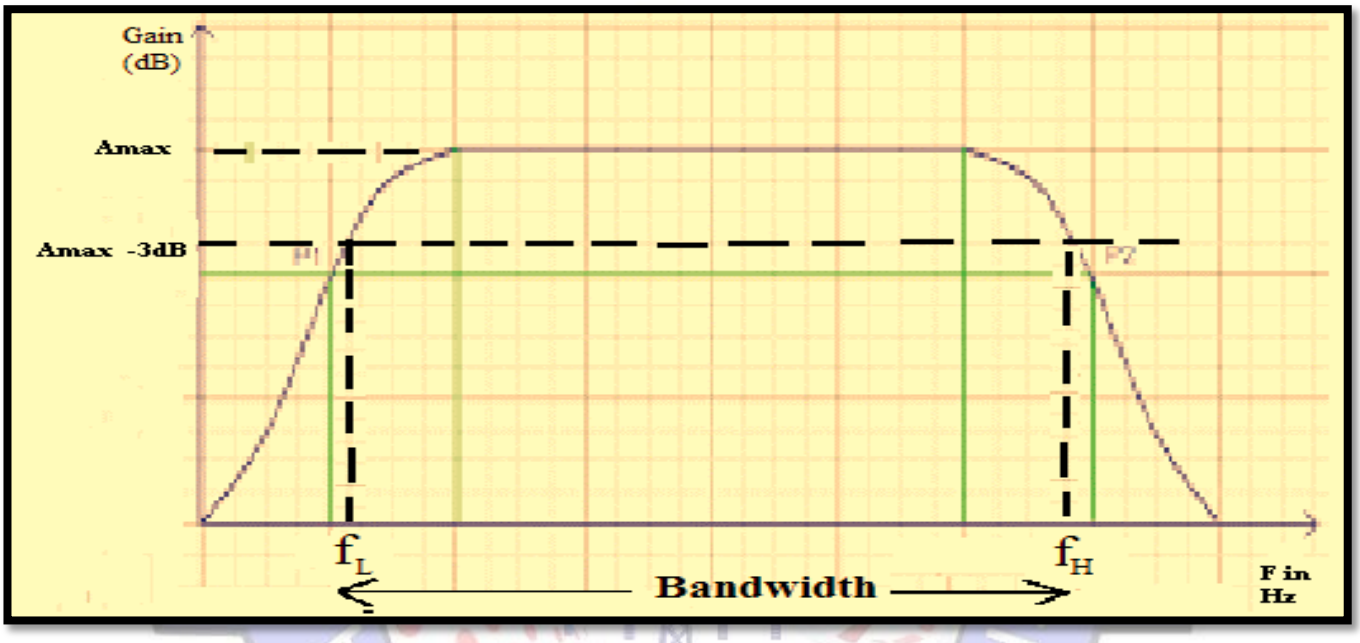
R2	R3	R4	R5	C1	C2	C3	VCC
4K7	39K	470Ω	3K3	100nF	1µf	100nF	15 V

2. Apply a sinusoidal signal to the input and dual- trace oscilloscope with one probe at the input and the other at the output.
3. Adjust the amplitude so that the output waveform has no distortion (The amplitude adjustment must be done in the mid band region). Set the input at a certain frequency of 10KHz and a level sufficient to give an output of 5 V_{PP} or 6 V_{PP}. Please note that the amplitude of the input signal will be kept constant during this experiment.



4. Move the specified frequency downward in steps of suitable amplitude. At each step check the input level and re-adjust it to the original value if needed, then measure and record the output amplitude. Keeping the input voltage constant, go on reducing the frequency until the output voltage reduces to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Lower Cut-off frequency (f_1).
5. Stop stepping when the output signal is below 1 V_{PP} from the original 5 V_{PP}or 6 V_{PP}.
6. Repeat for the interval of the specified frequency upwards, up to when the output voltage again reduces below 1Vpp. Keeping the input voltage constant, go on increasing the frequency until the output voltage decreases to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Upper Cut-off frequency (f_2).

7. Sketch the amplitude response as a function of the input signal frequency. (Use a semi-log graph paper, the frequencies are located on horizontal axis (log scale) and the amplitude is in dB located on the vertical axis (linear scale) as shown in figure 2. (Take extra points on the curve whenever you encounter a significant change in output while input is kept constant). Mark the -3dB cut-off points on the graph, which are the points where the gain becomes 0.703 times the center- band value (see figure).



8. Tabulate all the above data for steps 4 and 6 respectively.
   V_{in} =..... m V_{PP} volts.

Frequency (Hz)										
Output Voltage ($V_o$pp volts)										
Voltage Gain in decibels A_v =20log (V_o/V_i)										
Frequency (Hz)										
Output Voltage ($V_o$pp volts)										
Voltage Gain in decibels A_v =20log (V_o/V_i)										

Results

1. Maximum Voltage Gain (A_(max)) = ...
2. 3dB Lower cut off Frequency = ...
3. 3dB Upper cut off Frequency= .....
4. 3dB Bandwidth= .....
5. 3dB Gain= .....

Discussion

1. Discuss the influence of the bypass, coupling, internal, and stray capacitances on the frequency response.
2. List the types of coupling and which type of coupling was used in the experiment؟
3. Does CE have any effect on upper 3 dB point؟
4. What is meant by Bandwidth of an amplifier؟
5. The mid band gain of an amplifier is 100 and the lower cutoff frequency is 1KHz. Find the gain of the amplifier at a frequency of 20 Hz.
6. Why gain is constant in mid frequency region?

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Experimental Title: Operational Amplifier inverting and non-Inverting Characteristics.

1- OBJECTIVES:- To verify the performance of the operational amplifier in its linear range of operation, and investigate the causes of non-linear operation. In this lab session we build op amp circuits and carry out various calculations of op amp characteristics. At the end of this lab, we are to strengthen theoretical knowledge by gaining hands on experience of op-amp applications. This lab covers: Inverting Amplifiers and Non-inverting Amplifiers.

2- INTRODUCTION AND THEORY:-

Before jumping into op-amps, let's first go over some amplifier fundamentals. An amplifier has an input port and an output port. (A port consists of two terminals, one of which is usually connected to the ground node.) In a linear amplifier, the output signal = A × input signal, where A is the amplification factor or "gain." Depending on the nature of the input and output signals, we can have four types of amplifier gain: voltage gain (voltage out / voltage in), current gain (current out / current in), transresistance (voltage out / current in) and transconductance (current out / voltage in). Since most op-amps are voltage/voltage amplifiers, we will limit the discussion here to this type of amplifier. The circuit model of an amplifier is shown in Figure 1 (center dashed box, with an input port and an output port). The input port plays a passive role, producing no voltage of its own, and is modelled by a resistive element Ri called the input resistance. The output port is modelled by a dependent voltage source AVi in series with the output resistance Ro, where Vi is the potential difference between the input port terminals. Figure 1 shows a complete amplifier circuit, which consists of an input voltage source Vs in series with the source resistance Rs, and an output "load" resistance RL. From this figure, it can be seen that we have voltage-divider circuits at both the input port and the output port of the amplifier. This requires us to re-calculate Vi and Vo whenever a different source and/or load is used:

$$V_i = \left(\frac{R_i}{R_s + R_i}\right) V_s \qquad \text{.....(1)}$$

$$V_o = \left(\frac{R_L}{R_o + R_L}\right) A V_i \qquad \text{.....(2)}$$

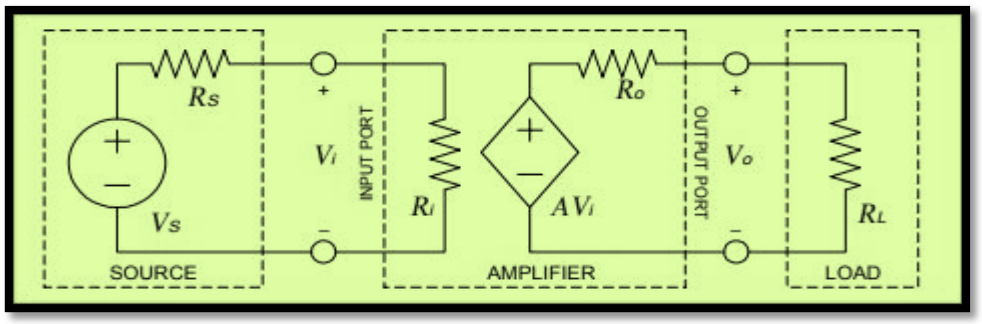


Figure 1: Circuit model of an amplifier circuit.

The amplifier model shown in Figure 1 is redrawn in Figure 2 showing the standard op-amp notation. An op-amp is a

"differential to single-ended" amplifier, i.e. it amplifies the voltage difference Vp – Vn = Vi at the input port and produces a voltage Vo at the output port that is referenced to the ground node of the circuit in which the op-amp is used.

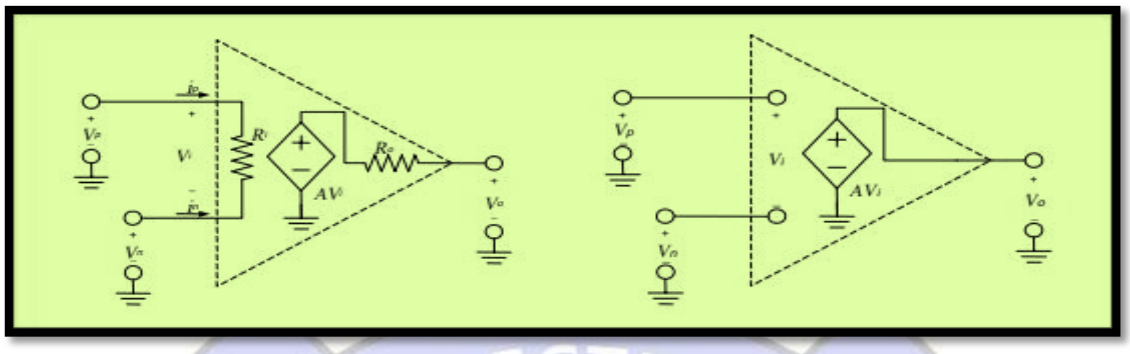


Figure 2: Standard op-amp

Figure 3: Ideal op-amp.

The ideal op-amp model was derived to simplify circuit analysis and is commonly used by engineers for first-order approximation calculations. The ideal model makes three simplifying assumptions:

Gain is infinite: $A = \infty$ (3)

Input resistance is infinite: $R_i = \infty$ (4)

Output resistance is zero: $R_o = 0$ (5)

Applying these assumptions to the standard op-amp model results in the ideal op-amp model shown in Figure 3. Because Ri = ∞ and the voltage difference Vp – Vn = Vi at the input port is finite, the input currents are zero for an ideal op-amp:

$$i_n = i_p = 0 \quad (6)$$

Hence there is no loading effect at the input port of an ideal op-amp:

$$V_i = V_s \quad (7)$$

In addition, because Ro = 0, there is no loading effect at the output port of an ideal op-amp:

$$V_o = A \times V_i \quad (8)$$

Finally, because A = ∞ and Vo must be finite, Vi = Vp – Vn = 0, or

$$V_p = V_n \quad (9)$$

Note: Although Equations 3-5 constitute the ideal op-amp assumptions, Equations 6 and 9 are used most often in solving op-amp circuits.

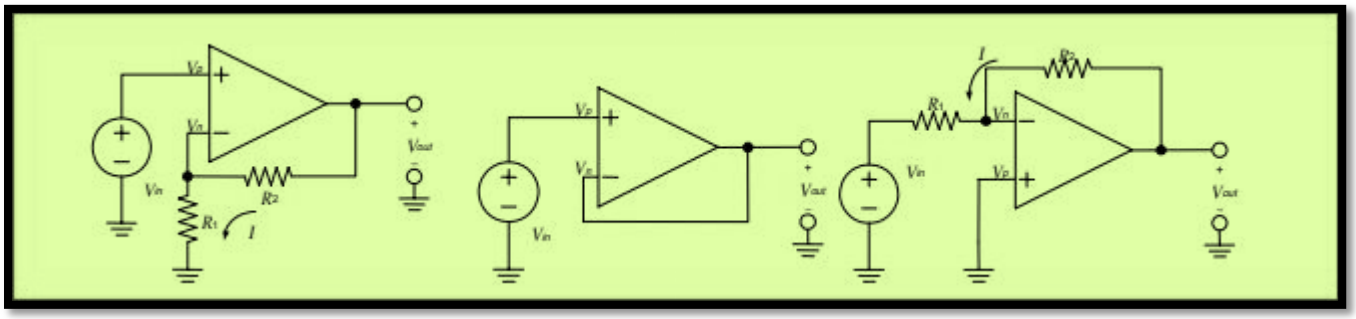


Figure 4a: Non-inverting amplifier *Figure 5a: Voltage follower* *Figure 6a: Inverting amplifier*

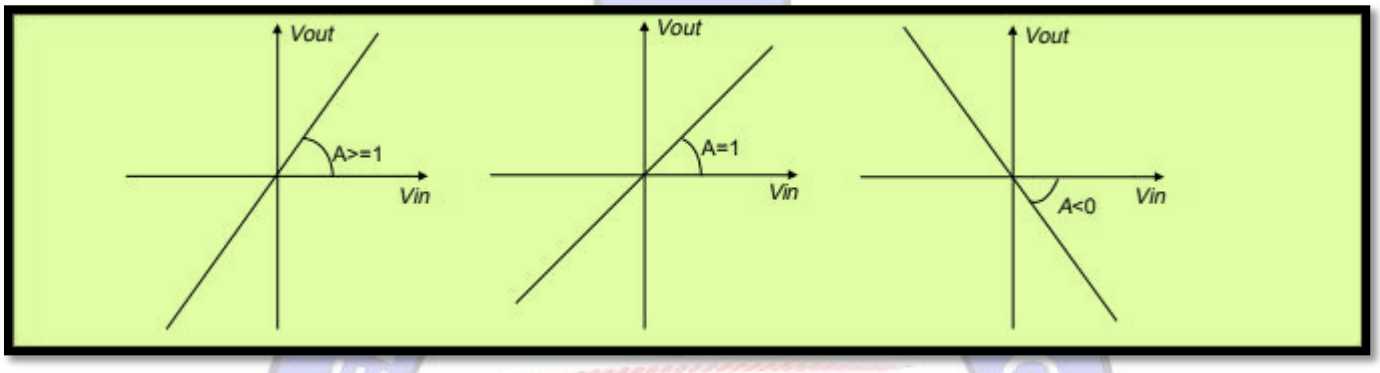


Figure 4b: Voltage transfer curve non-inverting amplifier *Figure 5b: Voltage transfer curve of voltage follower* *Figure 6b: Voltage transfer curve of inverting amplifier*

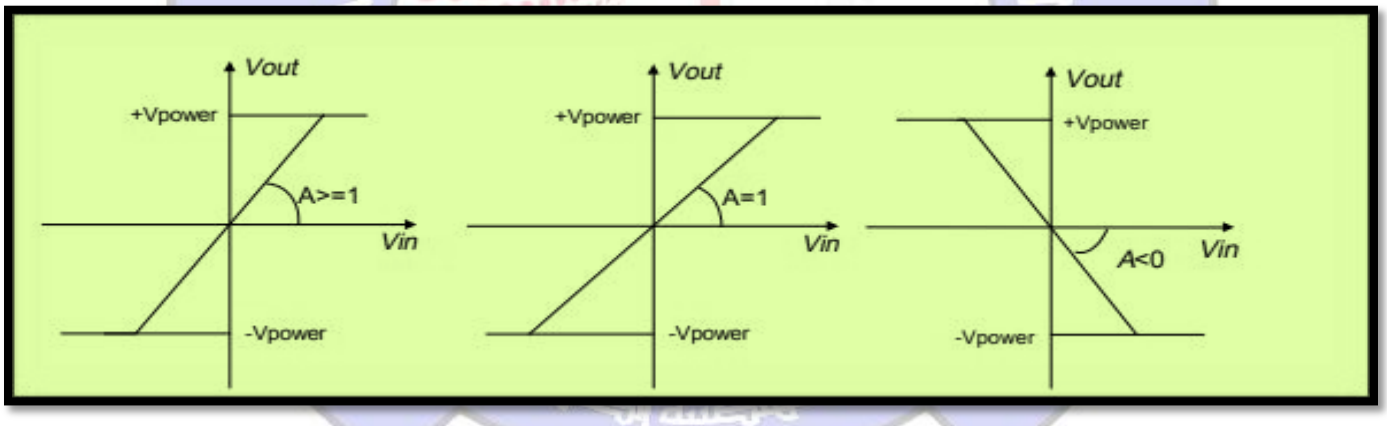
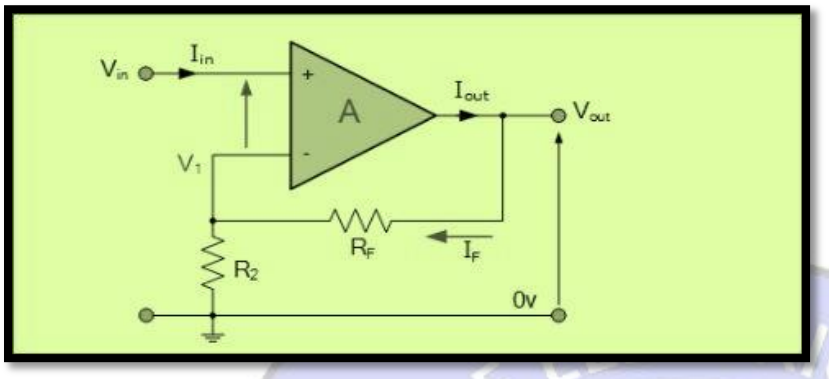


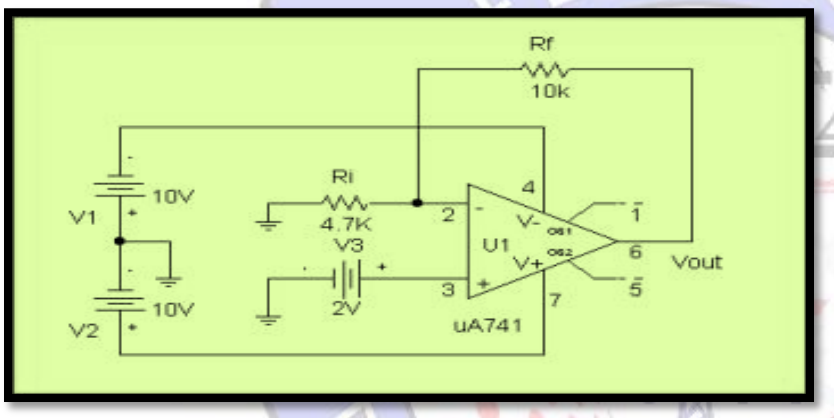
Figure 4c: Realistic transfer curve inverting amplifier *Figure 5c: Realistic transfer curve of voltage follower* *Figure 6c: Realistic transfer curve of non-of inverting amplifier*

Operational amplifier is one fundamental building block of analog circuits. When used properly in negative feedback configurations, the overall closed-loop transfer characteristic can be precisely set by stable passive components such as resistors, capacitors, and diodes, regardless of the potential variation of open-loop parameters. Negative feedback amplifier with op amp operating at its core provides key to highly reliable and stable analog functions. We will be simulating two basic configurations using the µA741 op amp. Note that the amplifier has two terminals labeled os1 and os2 besides the regular pins, and you can leave these two pins unconnected. (In case you are curious, these pins are used for offset adjustment for the op amp.)

Non-Inverting Amplifier: An ideal op-amp by itself is not a very useful device, since any finite non-zero input signal would result in infinite output. (For a real op-amp, the range of the output signal is limited by the positive and

negative power-supply voltages.) However, by connecting external components to the ideal opamp, we can construct useful amplifier circuits. Figure 4a shows a basic op-amp circuit, the non-inverting amplifier. The triangular block symbol is used to represent an ideal op-amp. The input terminal marked with a "+" (corresponding to Vp) is called the non-inverting input; the input terminal marked with a "–" (corresponding to Vn) is called the inverting input. To understand how the non-inverting amplifier circuit works, we need to derive a relationship between the input voltage Vin and the output voltage Vout. For an ideal op-amp, there is no loading effect at the input, so





$$V_p = V_i \qquad (10)$$

Since the current flowing into the inverting input of an ideal op-amp is zero, the current flowing through R1 is equal to the current flowing through R2 (by Kirchhoff's Current Law -- which states that the algebraic sum of currents flowing into a node is zero -- to the inverting input node). We can therefore apply the voltage-divider formula find Vn:

$$V_n = \left(\frac{R_1}{R_1 + R_2}\right) V_{out} \qquad (11)$$

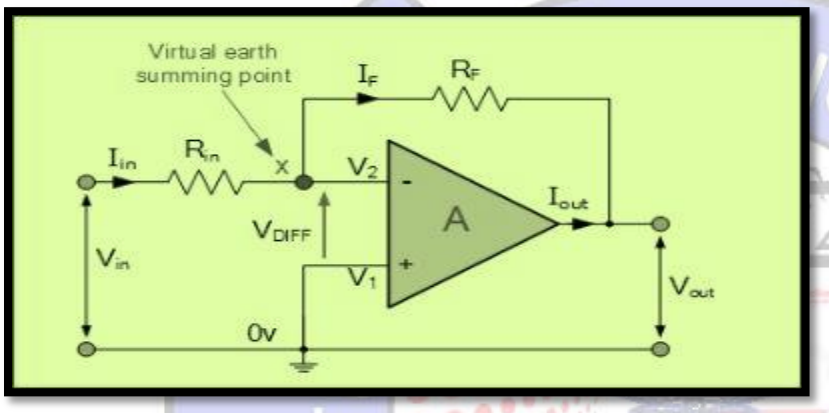
From Equation 9, we know that Vin = Vp = Vn, so

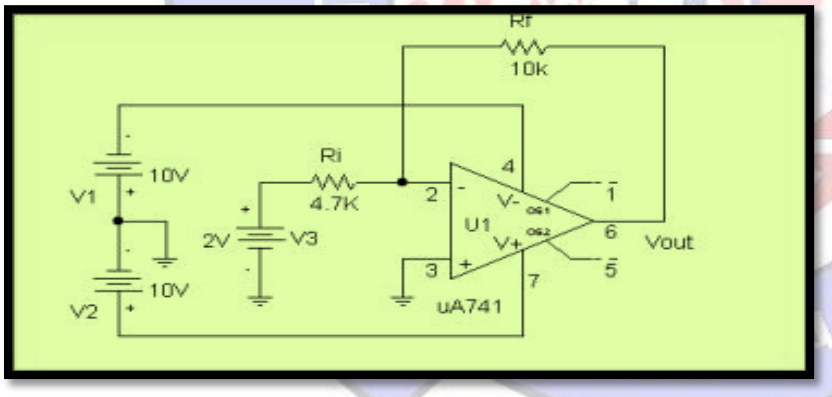
$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_{in} \qquad (12)$$

The voltage transfer curve (Vout vs. Vin) for a non-inverting amplifier is shown in Figure 4b. Notice that the gain (Vout / Vin) is always greater than or equal to one. The special op-amp circuit configuration shown in Figure 5a has a gain of unity, and is called a "voltage follower." This can be derived from the non-inverting amplifier by letting R1 =

∞ and R2 = 0 in Equation 12. The voltage transfer curve is shown in Figure 5b. A frequently asked question is why the voltage follower is useful, since it just copies input signal to the output. The reason is that it isolates the signal source and the load. We know that a signal source usually has an internal series resistance (Rs in Figure 1, for example). When it is directly connected to a load, especially a heavy (high conductance) load, the output voltage across the load will degrade (according to the voltage divider formula). With a voltage-follower circuit placed between the source and the load, the signal source sees a light (low conductance) load -- the input resistance of the op-amp. At the same time, the load is driven by a powerful driving source -- the output of the op-amp.

Inverting Amplifier Figure 6a shows another useful basic op-amp circuit, the inverting amplifier. It is similar to the non-inverting circuit shown in Figure 4a except that the input signal is applied to the inverting terminal via R1 and the non-inverting terminal is grounded. Let's derive a relationship between the input voltage Vin and the output voltage Vout. First, since Vn = Vp and Vp is grounded, Vn = 0. Since the current flowing into the inverting input of an ideal op-amp is zero, the current flowing through R1 must be equal in magnitude and opposite in direction to the current flowing through R2 (by Kirchhoff's Current Law):





$$\frac{V_{in}-V_n}{R_1}=\frac{V_{out}-V_n}{R_2} \qquad (13)$$

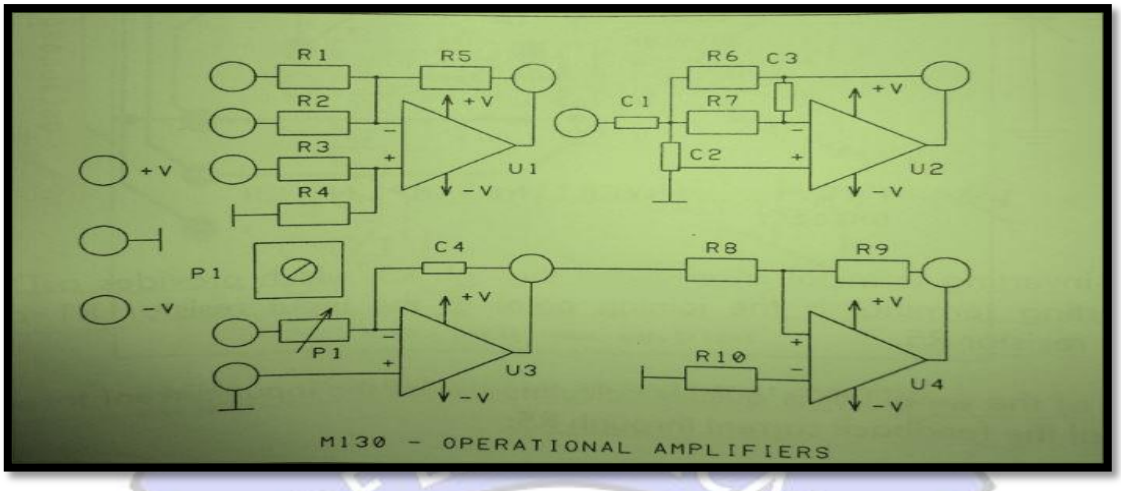
Since Vn = 0, we have:

$$V_{out}=\left(-\frac{R_2}{R_1}\right)V_{in} \qquad (14)$$

The gain of inverting amplifier is always negative, as shown in Figure 6b.

3- PROCEDURES:

The module M130 includes operational amplifier which can be configured in several manners.



Part 1: Inverting Amplifier, dc setting up

1- Apply a variable DC voltage at the input and the consequent output voltage is measured and recorded. Figure 7 shows the setup. Note that the M130 is power supplied at +15 and -15.

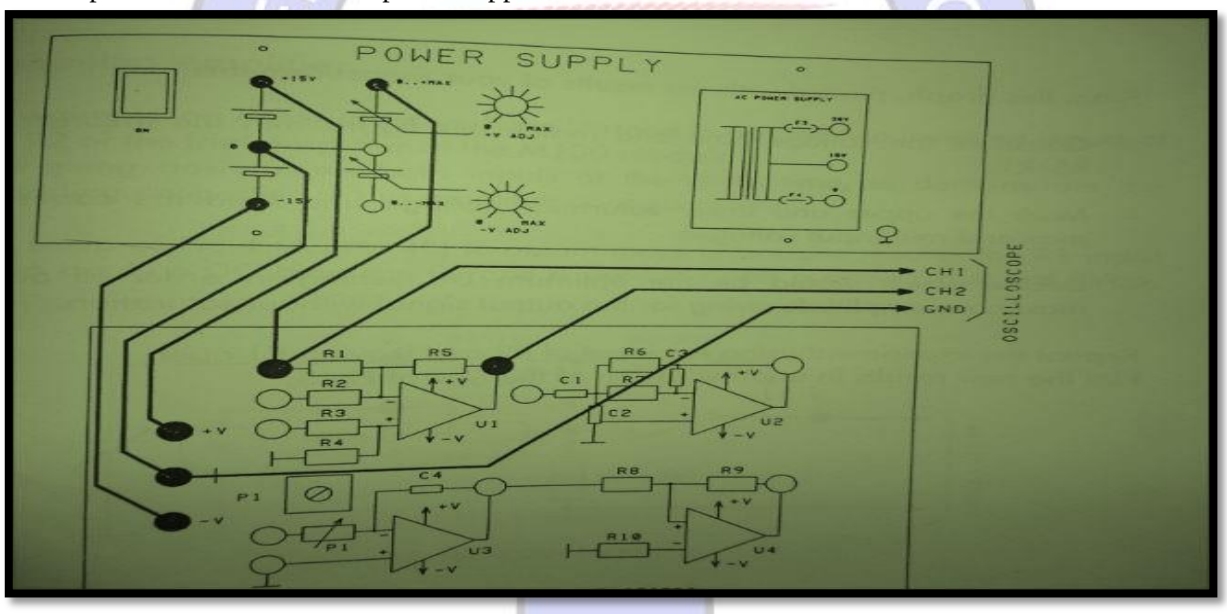
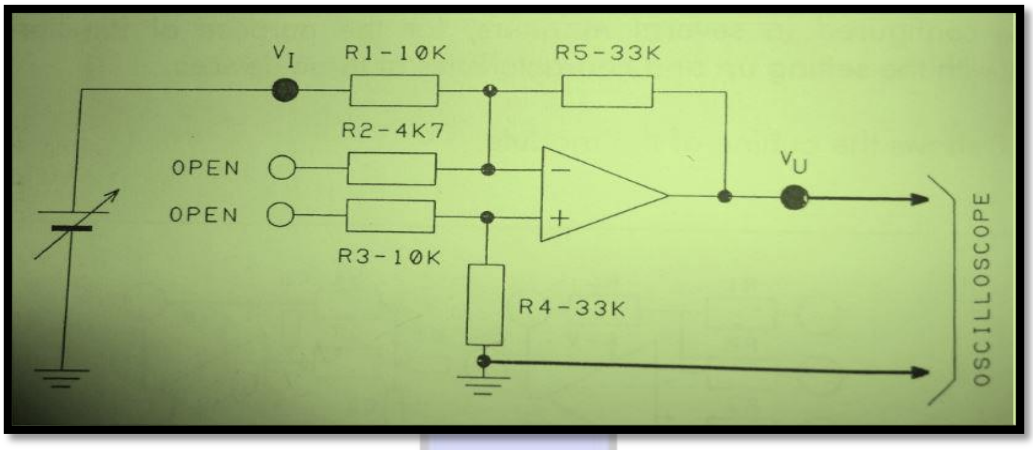


Figure 7



2- Repeat the experiment using the input R_2 and leaving R_1 open.

PART 2: Non- Inverting Amplifier, dc setting up

1- Apply a variable DC voltage at the input and the consequent output voltage is measured and recorded. Figure 8 shows the setup. Note that the M130 is power supplied at +15 and -15

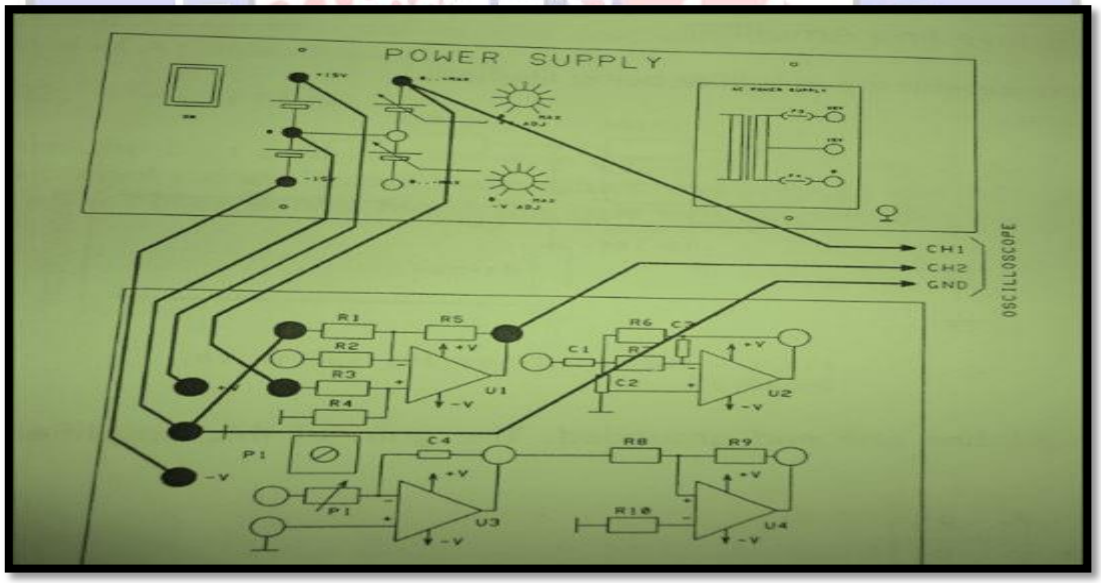
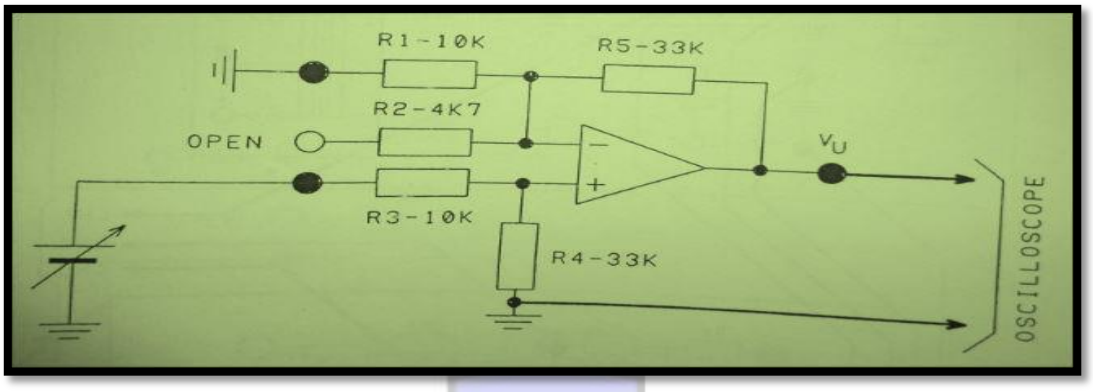


Figure 8



4- RESULTS:

PART 1

1- Record input and output characteristics. Plot the results of your measurements. The graph is between V_U and V_I values.
2- Mark the upper and lower saturation voltage and read the corresponding max and min input voltages.
3- Decide which would be the optimum DC setting in order to obtain the maximum amplitude swing for the output signal without saturation.
4- Repeat the requirements from 1 to 4 for step 2 in the procedures.

PART 2

1- Record input and output characteristics. Plot the results of your measurements. The graph is between V_U and V_I values.
2- Decide which would be the optimum DC setting in order to obtain the maximum amplitude swing for the output signal without saturation.
3- Find the phase relation between output and input.

5- Discussion:

1- For part1, Calculate the voltage gain and match it with the theoretical value $\frac{R_5}{R_1}$.

2- For part2, Calculate the voltage gain and match it with the theoretical value A= $\frac{R_4}{R_3 x\, R_4}(1 + \frac{R_5}{R_1})$.

Since $R_3 = R_1$ and $R_4 = R_5$, the formula becomes:

A= $\frac{R_5}{R_1 x\, R_5}(1 + \frac{R_1 + R_5}{R_1}) = \frac{R_5}{R_1}$.

University of Anbar
College of Engineering
Dept. of Electrical Engineering

Lab. Name: Electronic Lab./ 3rd Level
Experiment no.: 5
Lab. Supervisors: Mr. Hatem Al- Dulaimi,
Mr. Omar Al-Ani,
Mss. Mariam R. Mirza

EXPERIMENTAL TITLE: MULTISTAGE TRANSISTOR AMPLIFIERS.

1- OBJECTIVES:-

Often, a single stage transistor amplifier may not provide enough gain or input/output impedance for a desired application, to avoid this problem; we can use amplifier stages to form a multistage amplifier with the desirable gain or impedance properties.

2- INTRODUCTION AND THEORY:-

The output from a single stage amplifier is usually insufficient to drive an output device. In other words, the gain of a single amplifier is inadequate for practical purposes. Consequently, additional amplification over two or three stages is necessary. To achieve this, the output of each amplifier stage is coupled in some way to the input of the next stage. The resulting system is referred to as multistage amplifier. It may be emphasised here that a practical amplifier is always a multistage amplifier. For example, in a transistor radio receiver, the number of amplification stages may be six or more. In this chapter, we shall focus our attention on the various multistage transistor amplifiers and their practical applications. A transistor circuit containing more than one stage of amplification is known as multistage transistor amplifier. In a multistage amplifier, a number of single amplifiers are connected in cascade arrangement (The term cascaded means connected in series.) i.e. output of first stage is connected to the input of the second stage through a suitable coupling device and so on. The purpose of coupling device (e.g. a capacitor, transformer etc.) is (i) to transfer a.c. output of one stage to the input of the next stage and (ii) to isolate the d.c. conditions of one stage from the next stage. Fig. 5.1 shows the block diagram of a 3-stage amplifier. Each stage consists of one transistor and associated circuitry and is coupled to the next stage through a coupling device. The name of the amplifier is usually given after the type of coupling used. e.g.

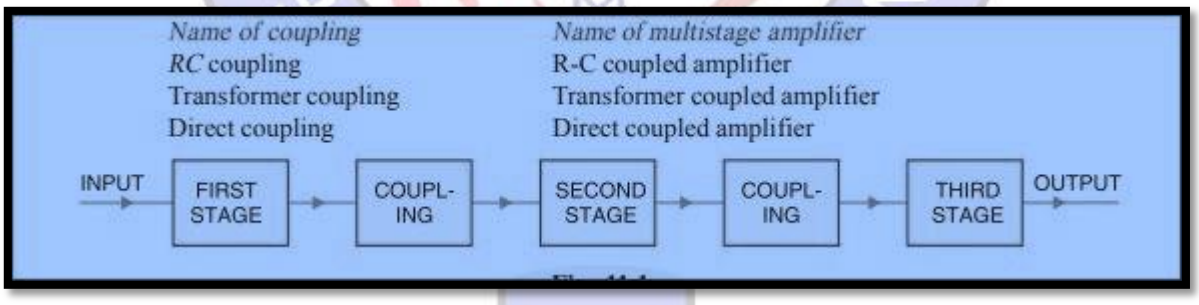


Figure 5-1

(i) In RC coupling, a capacitor is used as the coupling device. The capacitor connects the output of one stage to the input of the next stage in order to pass the a.c. signal on while blocking the d.c. bias voltages.

(ii) In transformer coupling, transformer is used as the coupling device. The transformer coupling provides the same two functions (viz. to pass the signal on and blocking d.c.) but permits in addition impedance matching.

(iii) In direct coupling or d.c. coupling, the individual amplifier stage bias conditions are so designed that the two stages may be directly connected without the necessity for d.c. isolation.

Regardless of the manner in which a capacitor is connected in a transistor amplifier, its behaviour towards d.c. and a.c. is as follows. A capacitor blocks d.c. i.e. a capacitor behaves as an "open to d.c. ($X_C = 1/2\pi fC$. For d.c., f = 0 so that $X_C \rightarrow \infty$. Therefore, a capacitor behaves as an open to d.c.)". Therefore, for d.c. analysis, we can remove the capacitors from the transistor amplifier circuit. A capacitor offers reactance (= $1/2\pi fC$) to a.c. depending upon the values of f and C. In practical transistor circuits, the size of capacitors is so selected that they offer negligible (ideally zero) reactance to the range of frequencies handled by the circuits. Therefore, for a.c. analysis, we can replace the capacitors by a short i.e. by a wire. The capacitors serve the following two roles in transistor amplifiers:

1. As coupling capacitors
2. As bypass capacitors .

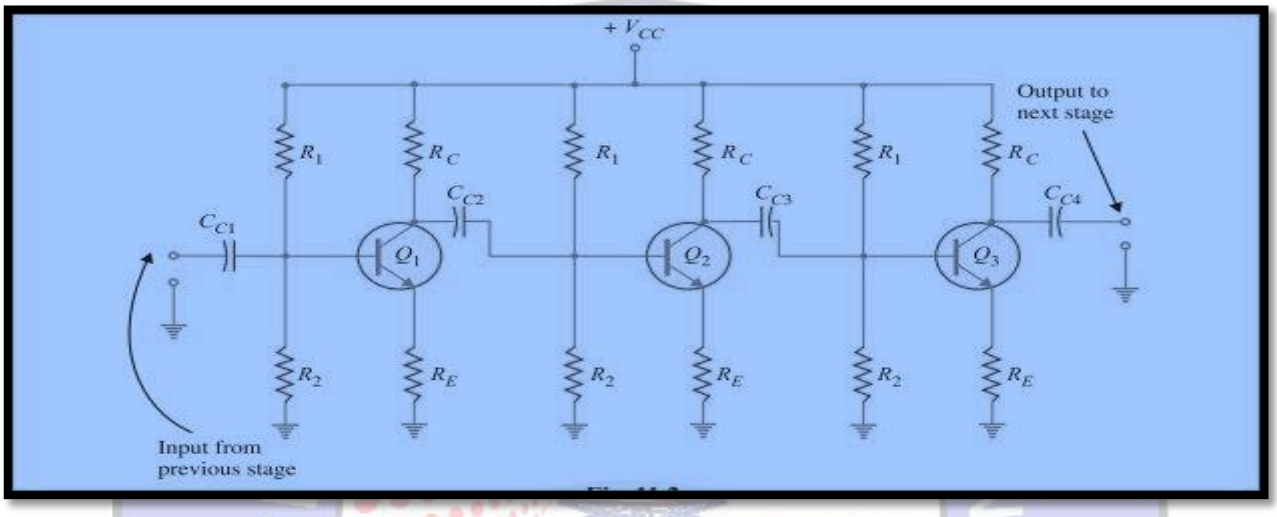


Figure 5-2

In the study of multistage amplifiers, we shall frequently come across the terms gain, frequency response and bandwidth. These terms stand discussed below:

(1) Gain. The ratio of the output *electrical quantity to the input one of the amplifier is called its gain.

The gain of a multistage amplifier is equal to the product of gains of individual stages. For instance, if G1, G2 and G3 are the individual voltage gains of a three-stage amplifier, then total voltage gain G is given by:

$$*G = G1 \times G2 \times G3$$

This can be easily proved. Supporse the input to first stage is V.

$$\text{Output of first stage} = G_1 V$$

$$\text{Output of second stage} = (G_1 V)\, G_2 = G_1 G_2 V$$

$$\text{Output of third stage} = (G_1 G_2 V) G_3 = G_1 G_2 G_3 V$$

$$\text{Total gain, } G = \frac{\text{Output of third stage}}{V}$$

or

$$G = \frac{G_1 G_2 G_3 V}{V} = G_1 \times G_2 \times G_3$$

*

It is worthwhile to mention here that in practice, total gain G is less than G1 × G2 × G3 due to the loading effect of next stages.

(2) Frequency response. The voltage gain of an amplifier varies with signal frequency. It is because reactance of the capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve between voltage gain and signal frequency of an amplifier is known as frequency response. Fig. 5.4 shows the frequency response of a typical amplifier. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at fr, called resonant frequency. If the frequency of signal increases beyond fr , the gain decreases

The performance of an amplifier depends to a considerable extent upon its frequency response. While designing an amplifier, appropriate steps must be taken to ensure that gain is essentially uniform over some specified frequency range. For instance, in case of an audio amplifier, which is used to amplify speech or music, it is necessary that all the frequencies in the sound spectrum (i.e. 20 Hz to 20 kHz) should be uniformly amplified otherwise speaker will give a distorted sound output.

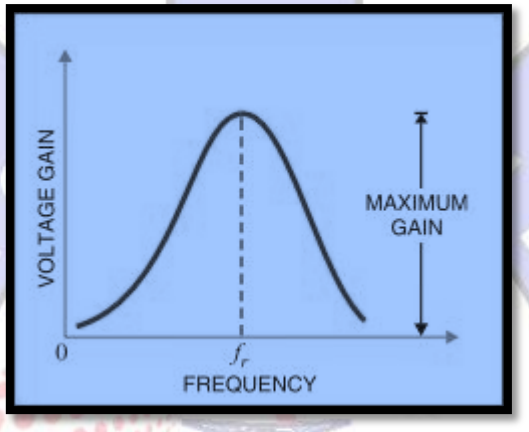


Figure 5-3

(3) Bandwidth. The range of frequency over which the voltage gain is equal to or greater than *70.7% of the maximum gain is known as bandwidth. The voltage gain of an amplifier changes with frequency. Referring to the frequency response in Fig. 5.4, it is clear that for any frequency lying between f1 and f2, the gain is equal to or greater than 70.7% of the maximum gain. Therefore, f 1 − f 2 is the bandwidth. It may be seen that f1 and f2 are the limiting frequencies. The former (f) is called lower cut-off frequency and the latter (f2) is known as upper cut-off frequency. For distortionless amplification, it is important that signal frequency range must be within the bandwidth of the amplifier.

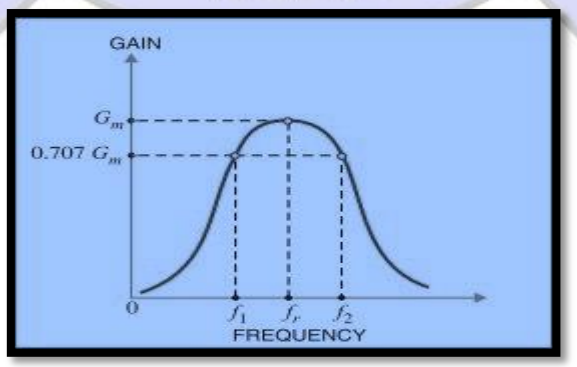


Figure 5-4.

RC Coupled Transistor Amplifier: This is the most popular type of coupling because it is cheap and provides excellent audio fidelity over a wide range of frequency. It is usually employed for voltage amplification. Fig. 5-5 shows two stages of an RC coupled amplifier. A coupling capacitor CC is used to connect the output of first stage to the base (i.e. input) of the second stage and so on. As the coupling from one stage to next is achieved by a coupling capacitor followed by a connection to a shunt resistor, therefore, such amplifiers are called resistance - capacitance coupled amplifiers. The resistances R1, R2 and RE form the biasing and stabilisation network. The emitter bypass capacitor offers low reactance path to the signal. Without it, the voltage gain of each stage would be lost. The coupling capacitor CC transmits a.c. signal but blocks d.c. This prevents d.c. interference between various stages and the shifting of operating point.

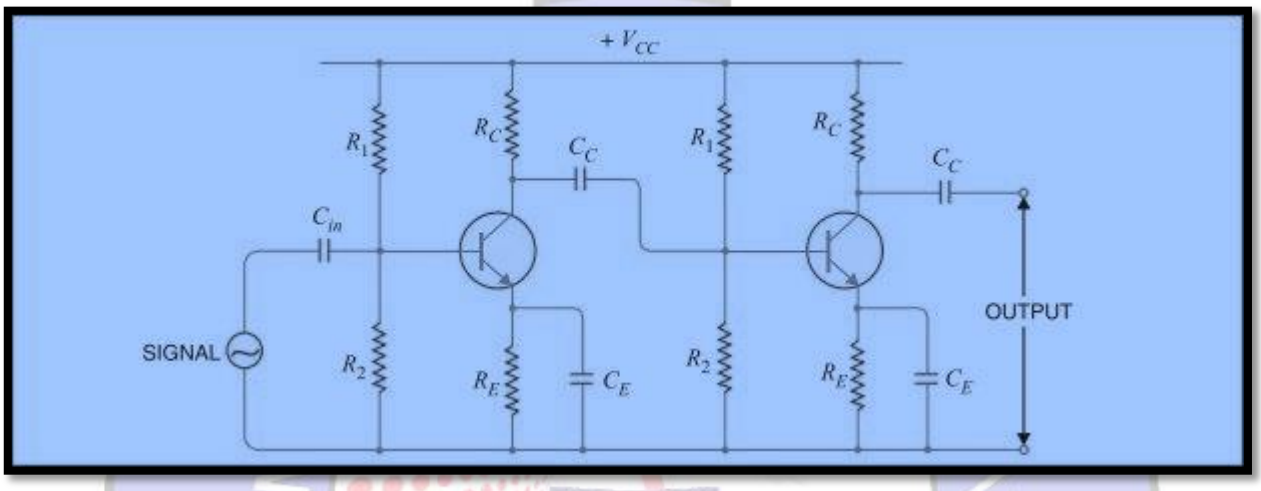


Figure 5-5.

Operation: When a.c. signal is applied to the base of the first transistor, it appears in the amplified form across its collector load RC. The amplified signal developed across RC is given to base of next stage through coupling capacitor CC. The second stage does further amplification of the signal. In this way, the cascaded (one after another) stages amplify the signal and the overall gain is considerably increased. It may be mentioned here that total gain is less than the product of the gains of individual stages. It is because when a second stage is made to follow the first stage, the effective load resistance of first stage is reduced due to the shunting effect of the input resistance of second stage. This reduces the gain of the stage which is loaded by the next stage. For instance, in a 3-stage amplifier, the gain of first and second stages will be reduced due to loading effect of next stage. However, the gain of the third stage which has no loading effect of subsequent stage, remains unchanged. The overall gain shall be equal to the product of the gains of three stages.

Frequency response. Fig.5-6 shows the frequency response of a typical RC coupled amplifier. It is clear that voltage gain drops off at low (< 50 Hz) and high (> 20 kHz) frequencies whereas it is uniform over mid-frequency range (50 Hz to 20 kHz). This behaviour of the amplifier is briefly explained below : (i) At low frequencies (< 50 Hz), the reactance of coupling capacitor CC is quite high and hence very small part of signal will pass from one stage to the next stage. Moreover, CE cannot shunt the emitter resistance RE effectively because of its large reactance at low frequencies. These two factors cause a falling of voltage gain at low frequencies. (ii) At high frequencies (> 20 kHz), the reactance of CC is very small and it behaves as a short circuit. This increases the loading effect of next stage and serves to reduce the voltage gain. Moreover, at high frequency, capacitive reactance of base-emitter junction is low which increases the base current. This reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency. (iii) At mid-frequencies (50 Hz to 20 kHz), the voltage gain of the amplifier is

constant. The effect of coupling capacitor in this frequency range is such so as to maintain a uniform voltage gain. Thus, as the frequency increases in this range, reactance of CC decreases which tends to increase the gain. However, at the same time, lower reactance means higher loading of first stage and hence lower gain. These two factors almost cancel each other, resulting in a uniform gain at mid-frequency.

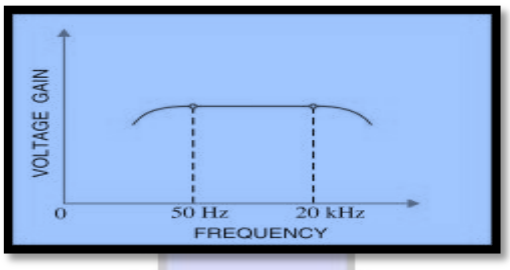


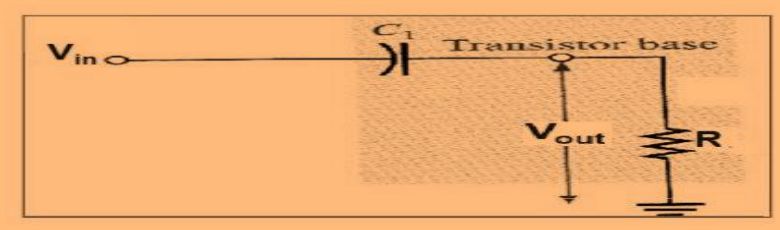
Figure 5-6.

Multistage Amplifiers: Frequency Response

$$V_o = \left(\frac{R}{R - jX_c}\right)V_{in}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{R}{R - j(1/\omega C)}$$

$$A_v = \frac{1}{1 - j(1/2\pi fCR)}$$



$$A_v = \frac{1}{1 - j(f_1/f)}$$
$$f_1 = 1/2\pi RC$$

$$A_v = \frac{1}{\sqrt{1 + (f_1/f)^2}} \angle \tan^{-1}(f_1/f)$$

Multistage Amplifiers: Low cut off Frequency

If n identical stages are connected together then overall voltage gain at lower frequency is given by:

$$A_{v\text{-low}} = A_{v1\text{-low}} \times A_{v2\text{-low}} \times A_{v3\text{-low}} \cdots\cdots\cdots \times A_{vn\text{-low}} = (A_{v\text{-low}})^n$$

where *n* is the number of cascaded stages. Since

$$A_{v1\text{-low}} = A_{v2\text{-low}} \cdots\cdots = A_{vn\text{-low}}$$

$$\left(\frac{A_{v-low}}{A_{v-mid}}\right)_{overall} = \left(\frac{A_{v-low}}{A_{v-mid}}\right)^n = \frac{1}{(1 - j(f_1/f)^n}$$

For lower cutoff frequency : $A_{v\text{-low}} / A_{v\text{-mid}})_{overall} = 1/\sqrt{2}$

$$\frac{1}{\sqrt{[1 + (f_1/f_{c-low})^2]^n}} = \frac{1}{\sqrt{2}}$$

$$f_{c-low} = \frac{f_1}{\sqrt{2^{\frac{1}{n}} - 1}}$$

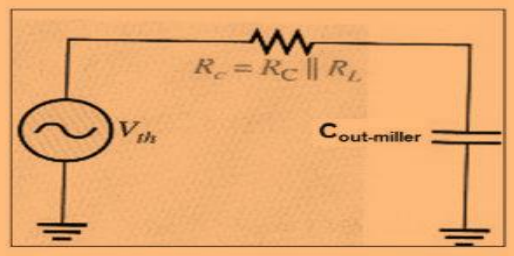
Multistage Amplifiers: High Cutoff Frequency

$$V_o = \left(\frac{-jX_c}{R-jX_c}\right)V_{in} \qquad A_v = \frac{V_{out}}{V_{in}} = \frac{1}{1+j(R\omega C)}$$

$$A_v = \frac{1}{1+j(2\pi fCR)} = \frac{1}{1+j(f/f_2)} \qquad A_v = \frac{1}{\sqrt{1+(f/f_2)^2}} \angle \tan^{-1}(f/f_2)$$

where $f_2 = 1/2\pi RC$

$$\left(\frac{A_{v-high}}{A_{v-mid}}\right)_{overall} = \left(\frac{A_{v-high}}{A_{v-mid}}\right)^n = \frac{1}{(1+j(f/f_2)^n}$$



For cutoff frequency : $A_{v\text{-}high} / A_{v\text{-}mid})_{overall} = 1/\sqrt{2}$

$$\frac{1}{\sqrt{[1+(f_{c-high}/f_2)^2]^n}} = \frac{1}{\sqrt{2}} \qquad f_{c-high} = f_2\sqrt{2^{\frac{1}{n}}-1}$$

Multistage Amplifiers: Frequency Response

The cutoff frequencies for cascaded amplifiers with identical values of f_{c1} and f_{c2} are found using

$$f_{c-low} = \frac{f_{c1}}{\sqrt{2^{\frac{1}{n}}-1}} \qquad f_{c-high} = f_{c2}\sqrt{2^{\frac{1}{n}}-1} \qquad BW_{overall} = f_{c-high} - f_{c-low}$$

where *n* is the number of cascaded stages.

When Each stage has a different lower & upper critical frequency

- When the lower critical frequency, f_{cL} , of each amplifier stage is different, the dominant lower critical frequency, f'_{cL} equals the critical frequency of the stage with the highest f_{cL}.
- When the upper critical frequency f_{cu}, of each amplifier stage is different, the dominant upper critical frequency f'_{cu}, equals the critical frequency of the stage with the lowest f_{cu}

3- PROCEDURES:

1- Build one of the possible circuits of dual-stage amplifiers shown in figures from 5-7 to 5- 12 using the following components listed in the table below, in addition use (P1 Trimmer 47K)if needed.

R1	R2	R3	R4	R5	R6	R7	R8	R9	C1	C2	C3	C4	C5	Q1	Q2
22K	4K7	39K	470Ω	3K3	2K7	10K	1K5	3K3	100nF	1μF	100nF	1μF	100nF	BC337	BC337

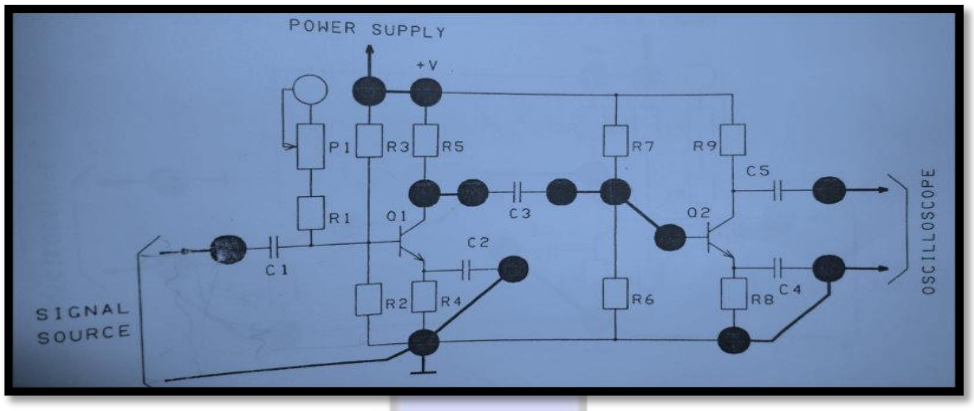


Figure 5-7

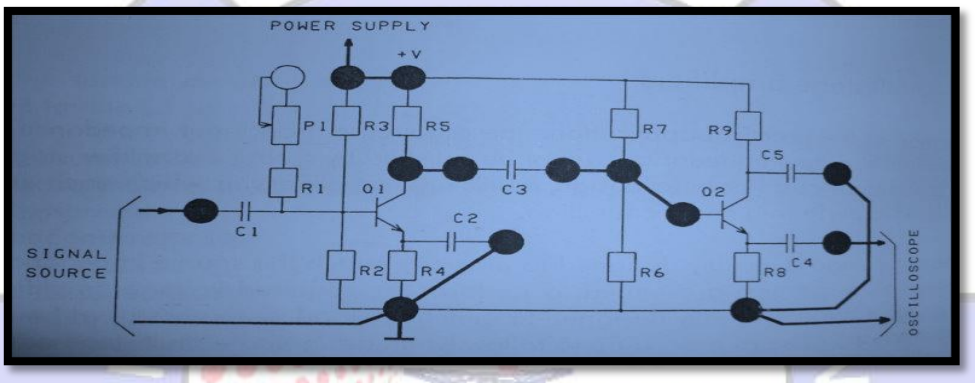


Figure 5-8

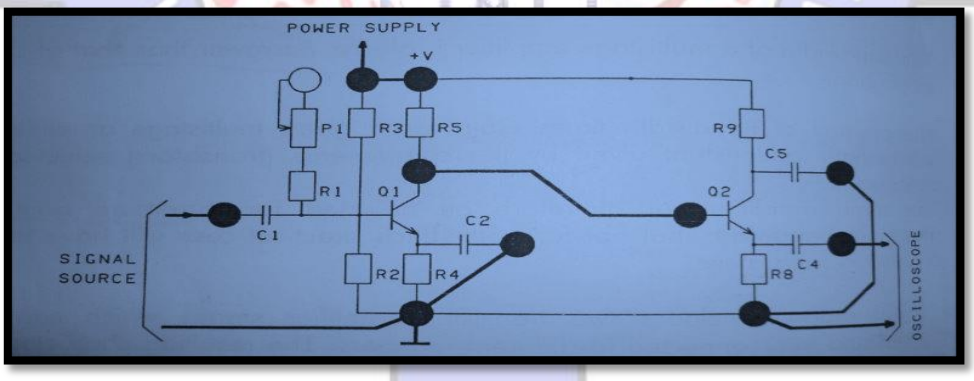


Figure 5-9

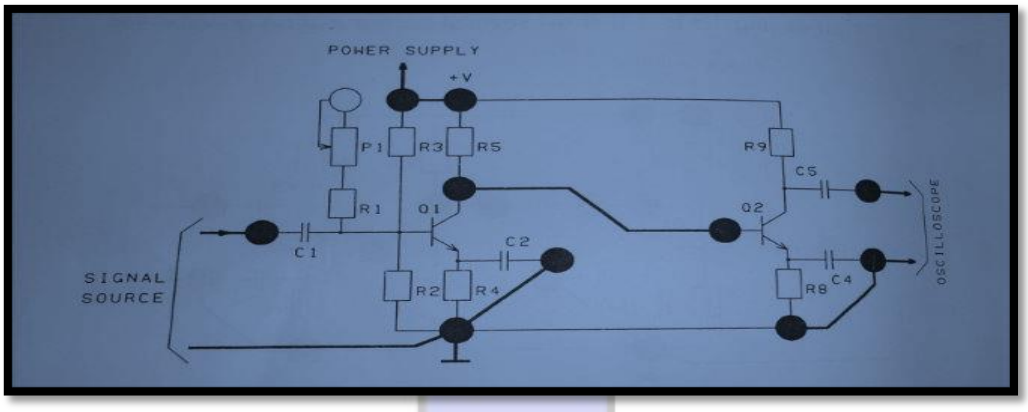


Figure 5-10

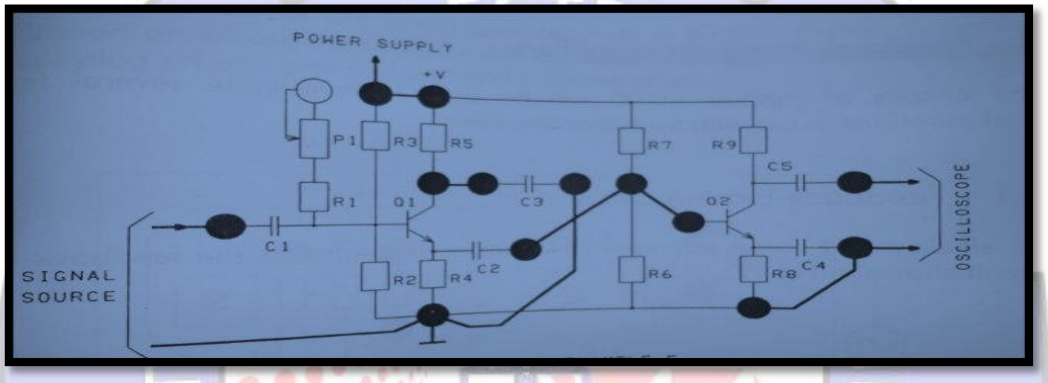


Figure 5-11

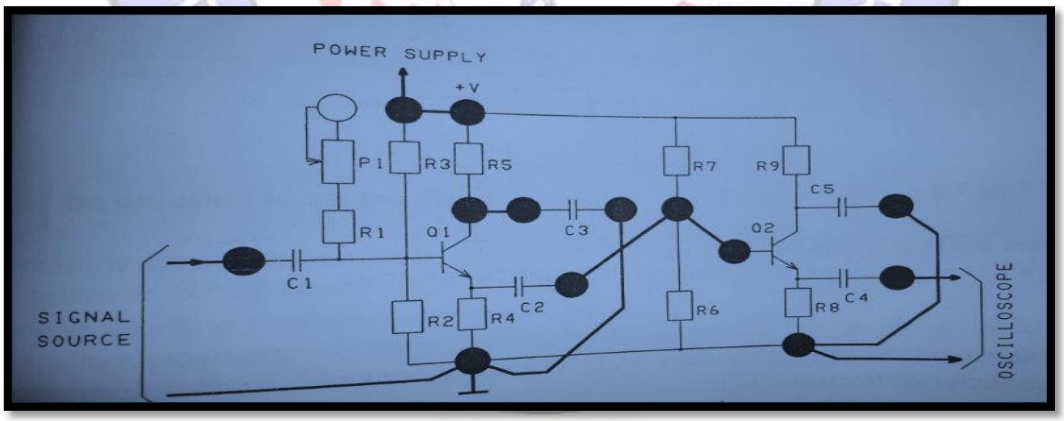


Figure 5-12

2- Apply a sinusoidal signal to the input and dual- trace oscilloscope with one probe at the input and the other at the output.

3- Adjust the amplitude so that the output waveform has no distortion (The amplitude adjustment must be done in the midband region). Set the input at a certain frequency of 10KHz and a level sufficient to give an output of 5Vpp or 6 Vpp. Please note that the amplitude of the input signal will be kept constant during this experiment.

4- Move the specified frequency downward in steps of suitable amplitude. At each step check the input level and re-adjust it to the original value if needed, then measure and record the output amplitude. Keeping the input voltage constant, go on reducing the frequency until the output voltage reduces to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Lower Cut-off frequency (*f1*).

5- Stop stepping when the output signal is below 1Vpp from the original 5Vpp or 6Vpp.

6- Repeat for the interval of the specified frequency upwards, up to when the output voltage again reduces below 1Vpp. Keeping the input voltage constant, go on increasing the frequency until the output voltage decreases to 0.707 times its value at 10 KHz. The frequency at which this happens gives you the Upper Cut-off frequency (*f2*).

7- Sketch the amplitude response as a function of the input signal frequency. (Use a semi-log graph paper, the frequencies are located on horizontal axis (log scale) and the amplitude is in dB located on the vertical axis (linear scale) as shown in figure 2. (Take extra points on the curve whenever you encounter a significant change in output while input is kept constant). Mark the -3dB cut-off points on the graph, which are the points where the gain becomes 0.703 times the center- band value.

8- Tabulate all the above data for steps 4 and 6 respectively.

Vin=…… **mVpp** volts.

Frequency(Hz)										
Output Voltage ($V_o$pp volts)										
Voltage Gain in decibels $A_v = 20\log(V_o/V_i)$										

Frequency(Hz)										
Output Voltage ($V_o$pp volts)										
Voltage Gain in decibels $A_v = 20\log(V_o/V_i)$										

4- RESULTS:

1. Maximum Voltage Gain (A_{max})= .....
2. 3dB Lower cut off Frequency = ...
3. 3dB Upper cut off Frequency= .....
4. 3dB Bandwidth= .....
5. 3dB Gain= .....

5- Discussion:

1- Why there is a need to construct multistage amplifiers.

2- What are the advantages, disadvantages and applications of RC- coupled amplifiers.

3- Why do you prefer to express the gain in db.

4- If different types of coupling are compared as shown in the table below:

S. No	Particular	*RC* coupling	Transformer coupling	Direct coupling
1.	*Frequency response*	Excellent in the audio frequency range	Poor	Best
2.	*Cost*	Less	More	Least
3.	*Space and weight*	Less	More	Least
4.	*Impedance matching*	Not good	Excellent	Good
5.	*Use*	For voltage amplification	For power amplification	For amplifiying extremely low frequencies

Why does transformer coupling give poor frequency response?

5- What is the difference between cascode amplifiers and cascade multistage amplifier? Explain your answer with the aid of block diagrams.

6- Compare the voltage gain between single stage amplifier and multistage amplifier from the obtained results.

Notes:

Points to ponder:

a.) Impedance Matching.
When coupling amplifier stages together impedance matching is important so that as much signal as possible is transferred from the output of one stage to the input of the next, keeping inter stage losses to a minimum.

b.) Correct Frequency Response.
Ensuring that the correct bandwidth is maintained throughout all stages of amplification.

c.) DC Isolation.
Whether it is required or not. It may be required that where the output of one stage is at a different DC potential to the input of the next, the two stages are electrically isolated from each other.

University of Anbar
College of Engineering
Dept. of Electrical Engineering

Lab. Name: Electronic Lab./ 3rd Level
Experiment no.: 6
Lab. Supervisors: Mr. Hatem Al- Dulaimi,
Mss. Mariam R. Mirza,
Mr. Omar Al-Ani

Experimental Title: Summing Amplifier

1- OBJECTIVES:- Study of Operational Amplifier as a Summing Amplifier.

2- INTRODUCTION AND THEORY:-

Operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage. The output stage is generally a push-pull or push-pull complementary symmetry pair. An operational amplifier is available as a single integrated circuit package. The operational amplifier is a versatile device that can be used to amplify DC as well as AC input signals and was originally designed for performing mathematical operations such as addition, subtraction, multiplication, and integration. Thus the name operational amplifier stems from its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications, such as AC and DC signal amplification, active filters, oscillators, comparators, regulator, regulators, and others. The op-amp may be used as an Adder or Scalar in both inverting as well as non-inverting configuration figure 1 shows the inverting configuration with three inputs Input 1, Input 2 and Input 3. Depending on the relationship between the feedback resistor Rf and the input resistor Ra, Rb, and Rc, the circuit can be used as a summing amplifier (Adder) or a scaling amplifier. The circuit's function can be verified by examining the expression for the output voltage, Vout.

$$V_{out} = -[(R_F / R_a)V_a + (R_F / R_b)\, V_b + (R_F / R_c)\, V_c)] \ldots\ldots (1)$$

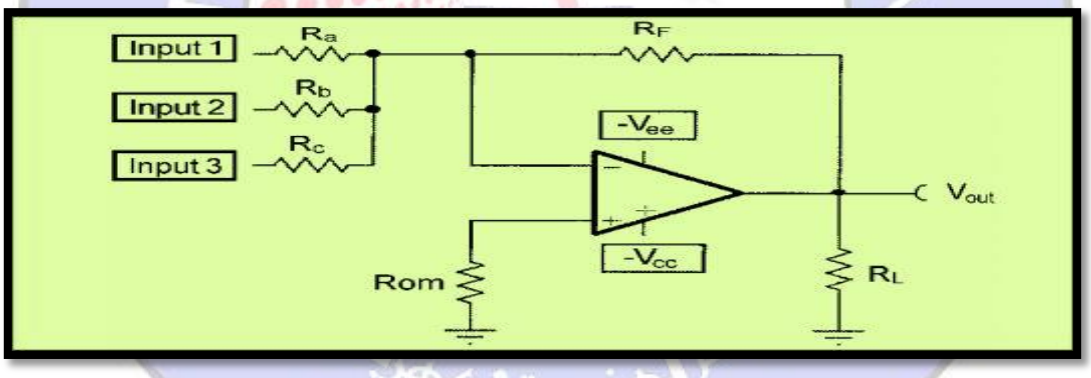


Figure 1

Summing Amplifier: If in the circuit of figure 1, Ra = Rb = Rc = R, then equation 1 can be rewritten as:

$$V_{out} = -(R_F / R) * (V_a + V_b + V_c) \qquad \ldots\ldots (2)$$

This means that the output voltage is equals to the negative sum of all the inputs times the gain of the circuit RF / R; hence the circuit is called a Summing amplifier, obviously, when the gain of the circuit is 1, that is Ra = Rb = Rc = RF, the output voltage is equal to the negative sum of all input voltages. Thus:

$$V_{out} = -(V_a + V_b + V_c) \qquad \ldots\ldots (3)$$

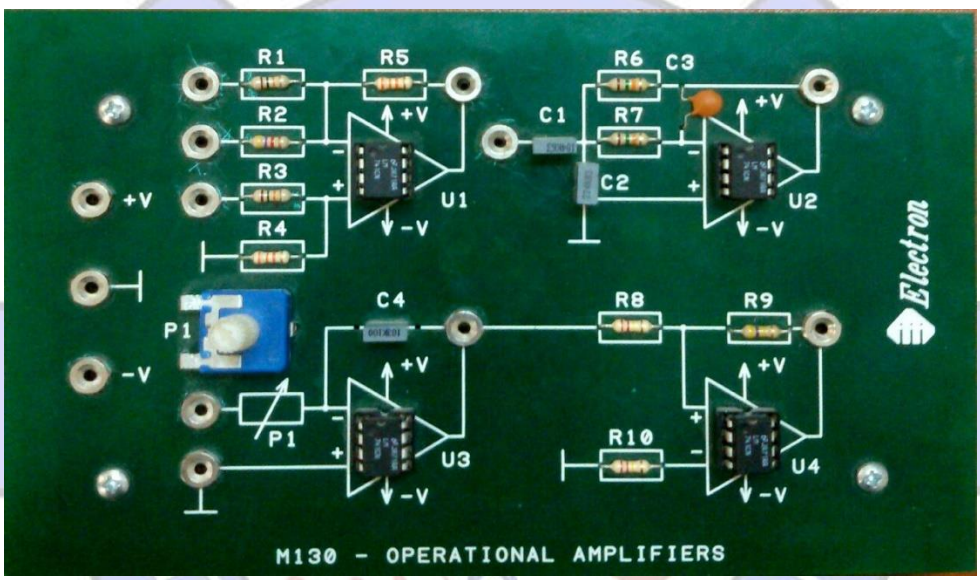
Scaling or Weighted amplifier: If each input voltage is amplified by a different factor, in other words, weighted differently at the output, the circuit in figure 1 is then called a scaling or weighted amplifier. This condition can be accomplished if Ra, Rb, and Rc are different in values. Thus the output voltage of the scaling amplifier is:

$$V_{out} = -[(R_F / R_a) V_a + (R_F / R_b) V_b + (R_f / R_c) V_c] \quad \ldots\ldots (4)$$

Where RF/Ra ≠RF/Rb ≠RF/Rc

3- PROCEDURES:

The module M130 includes operational amplifier which can be configured in several manners. We are going to use both inputs at the same time, to demonstrate the signal- adding properties of this amplifier configuration.



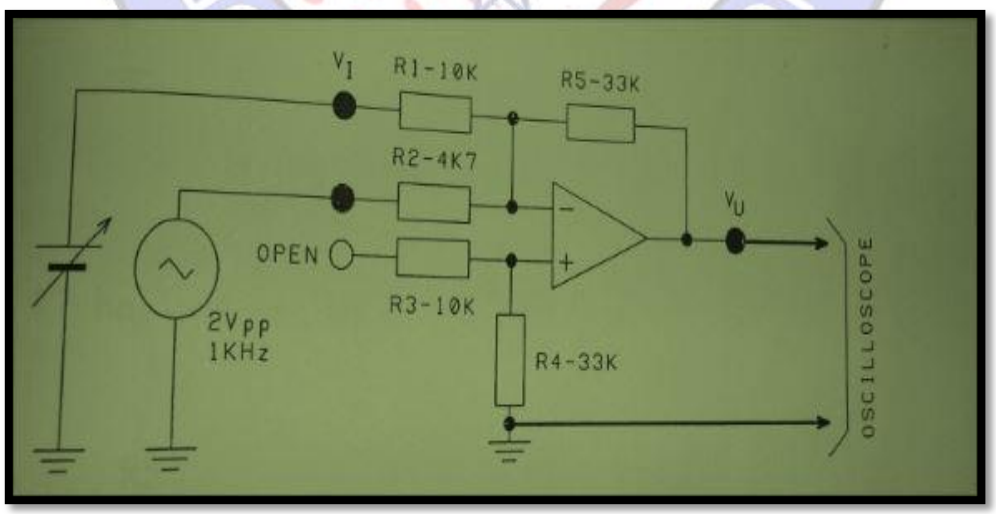


Figure 4-A: Setup of the experiment

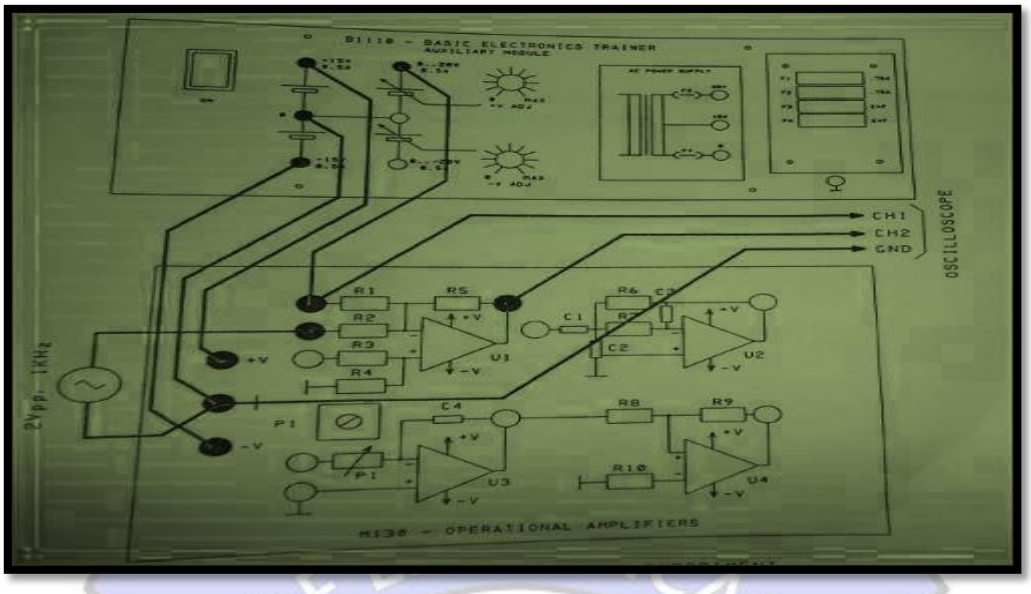


Figure 4-B: Practical wiring for the experiment

1- Apply a variable DC voltage at the input and the consequent output voltage is measured and recorded. Figure 4-A and 4-B shows the setup. Note that the M130 is power supplied at +15 and -15.

2- The R1 input is used to apply a DC bias, the R2 one is used to apply a sinewave signal 2Vpp, 1 KHz.

3- Adjust the bias and the sinewave amplitude in order to obtain the max undistorted output swing.

4- Swap the R1 and R2 input sources and repeat your observations.

4- RESULTS:

1- Record the output sinewave and the output DC level at step 2 from the procedures.
2- Record the values at step 3 from the procedures.
3- Repeat the required records at step 1 and 2 for step 4 from the procedures.

5- Discussion:-

1-Calculate the voltage gain and match it with the theoretical value A2= $\frac{R_5}{R_2}$, A1= $\frac{R_5}{R_1}$.

2-What are the applications of summing amplifiers? Briefly explain them.

University of Anbar
College of Engineering
Dept. of Electrical Engineering

Experimental Title: Differential Amplifier

1- OBJECTIVES:- Differential amplifiers are designed to amplify the difference between two signals. Differential amplifiers are thereby able to reduce noise that is common to both inputs, only amplifying the differential signal that we're interested in. We can quantify the differential-mode versus common-mode gain in a quantity called the common-mode rejection ratio (CMRR). Differential amplifiers also lend themselves to use in feedback, though we will not explore that usage in this lab. A typical differential amplifier with a single-ended output that you are familiar with is the op-amp.

2- INTRODUCTION AND THEORY:-

The differential amplifier basically is the operational amplifier already used for the preceding experiment figure 1, this time wired in a manner so that both the inverting input at R1 and the non-inverting one at R3 are used. The result is that the output signal is the linear subtraction of the two input signals, each one multiplied by the relevant gain:

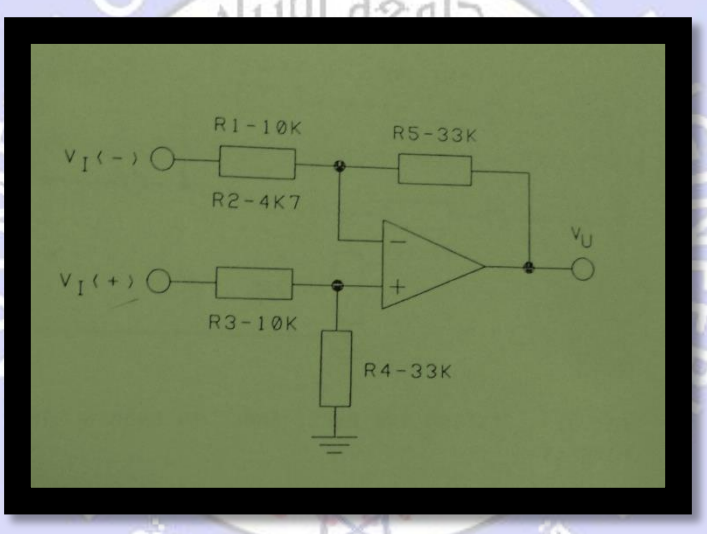


Figure 1: The differential amplifier

$V_U = V_{i(+)} \times A_{(+)} - V_{i(-)} \times A_{(-)}$

Since we already discussed and measured the A(+) and A(-) gains, we know that: $A_{(+)} = A_{(-)} = \frac{R5}{R1}$

This allows us to write: $V_U = A(V_{i(+)} - V_{i(-)})$

This means that the amplifier amplifies the difference between the signals applied at the inputs. This amplifier is often used as an instrumentation amplifier.

We shall practically test the deferential amplifier in a rather unusual way, but a very effective one: since the differential amplifier amplifies the difference $V_{i(+)} - V_{i(-)}$, we will apply the same signal for $V_{i(+)}$ and $V_{i(-)}$ and shall verify that the output is a null signal.

The quality of the difference amplifier is expressed in terms of a quantity called the Common Mode Rejection Ratio (CMRR). The CMMR of a differential amplifier is defined by the ratio

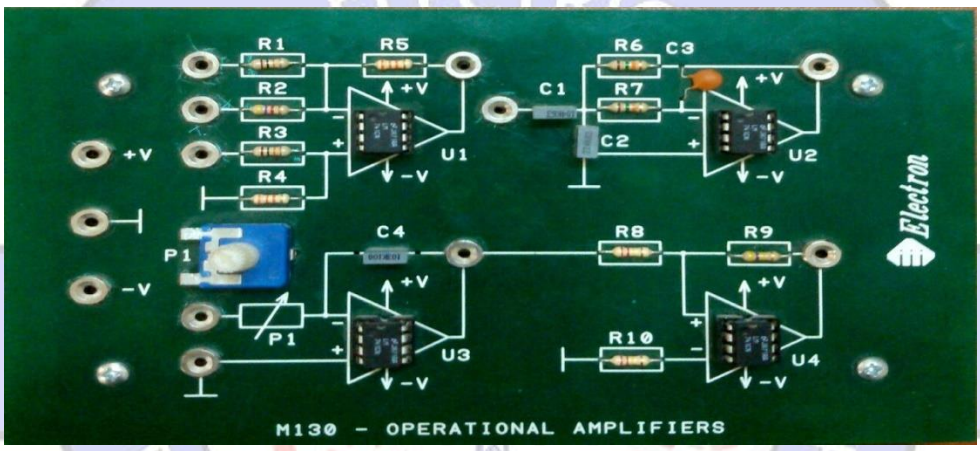
$$\text{CMRR} = \frac{\text{differential gain}}{\text{common mode gain}}$$

Where the common mode gain is given by

$$A_{cm} = \frac{v_o}{\frac{(v_1 + v_2)}{2}}$$

3- PROCEDURES:

The module M130 includes operational amplifier.



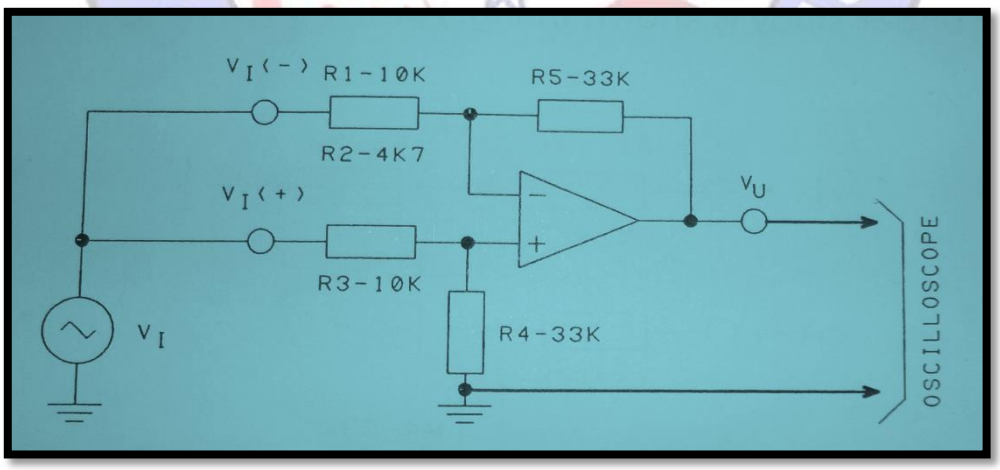


Figure 2 -A: Setup of the experiment

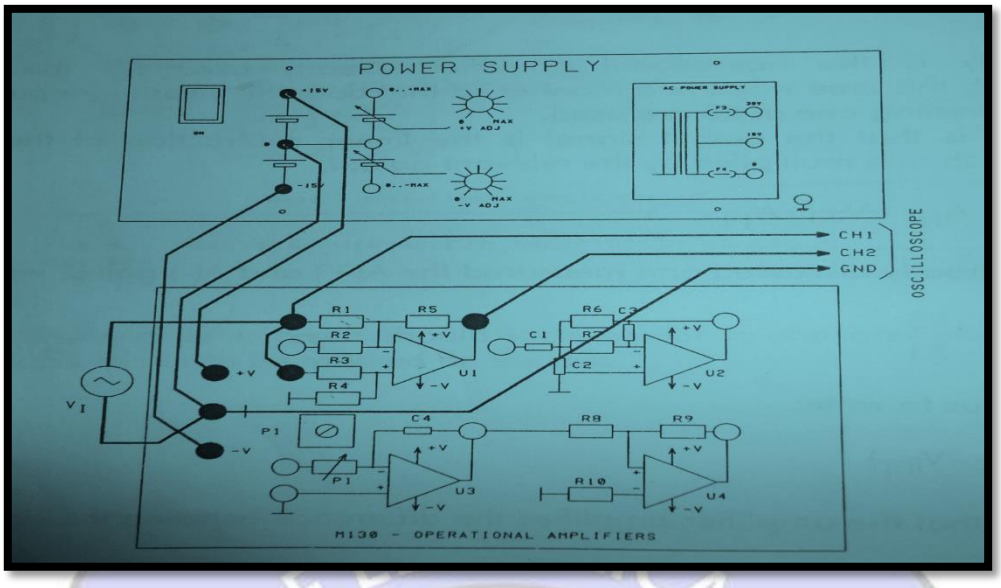


Figure 2-B: Practical wiring for the experiment

1-Apply a sine wave input signal for instance, a 1 to 10 Vpp at 1 KHz and observe the output. The oscilloscope is used to display this signal at CH1 (trigger on CH1) and the output signal at CH2. Note that the M130 is power supplied at +15 and -15.

2- Measure the gain V_o/V_2 (when $V_1 = 0$), at 100 Hz, 1 kHz, and 10 kHz, 20 kHz, and 100 kHz. *(Note the gain measurements should include the phase as well).* What is the gain at low frequencies? Why is the gain lower than expected at high frequencies?

3. Now measure V_o/V_1 when $V_2=0$ at 1 kHz. Be sure to observe and record the phase of the output as compared to the input.

4. Measure the common mode ($V_1=V_2$) voltage gain and phase, describe your method and results.

4- RESULTS:

1- Calculate common mode rejection ratio parameter CMRR which is usually expressed as:

CMRR= $20\log_{10}\frac{V_O}{V_i}$

5- Discussion:-

1- What are the applications of differential amplifiers?

2- Define common mode rejection ratio (CMRR). Give its significance in device performance.

3- Compare between instrumentation amplifier and differential amplifier.

University of Anbar
College of Engineering
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Lab. Name: Electronic Lab./ 3rd Level
Experiment no.: 8
Lab. Supervisors: Mr. Hatem Al- Dulaimi,
Mss. Mariam R. Mirza,
Mr. Omar Al-Ani

Experimental Title: The band pass active filter

1- OBJECTIVES:-

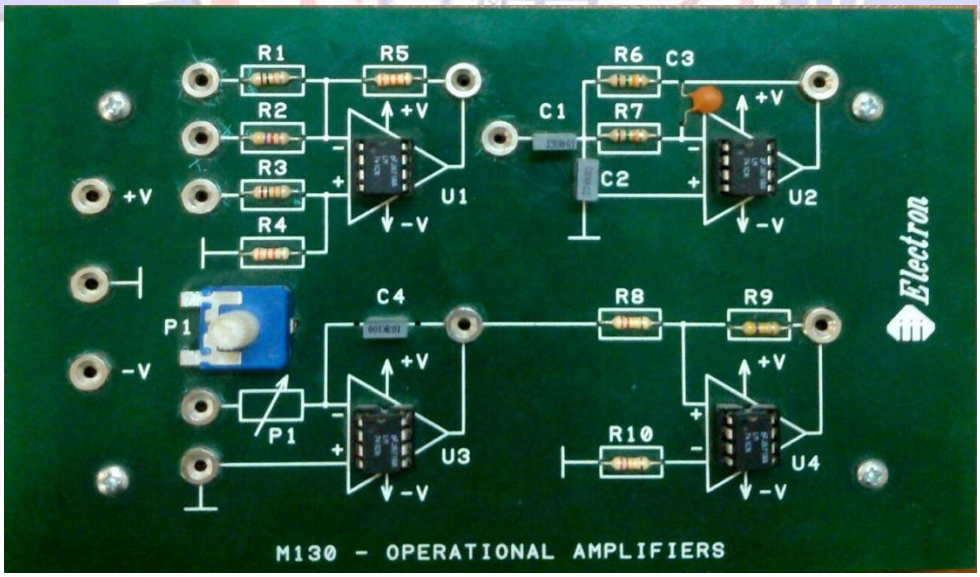
To demonstrate the work of band pass active filter.

2- INTRODUCTION AND THEORY:-

The band pass filter takes advantage of the low pass configuration as well as the high pass configuration. The two of these combine to for a range of frequencies that is called the pass band. Below the lower cutoff frequency the signals are stopped as well as above the higher cutoff frequency. The difference between these two frequencies is called the bandwidth of the filter. The logic behind the cutoff frequencies is a little misleading. The lower cutoff frequency is controlled by the high pass filter part of the band pass filter. On the same type of idea, the upper cutoff frequency is controlled by the low pass filter part of the band pass filter. The circuit shown in Figure 6 is that of a basic pass band filter. Notice the combination of the low pass and high pass connections. The combination of a 1st order HP and a 1st order LP creates a 2nd order band pass. If the trend were to continue a 2nd order HP and a 2nd order LP create a 4th order band pass.

3- PROCEDURES:

The module M130 includes an example of BP active filter, as depicted in figure 1, figure 2 shows the practical setup of the experiment.



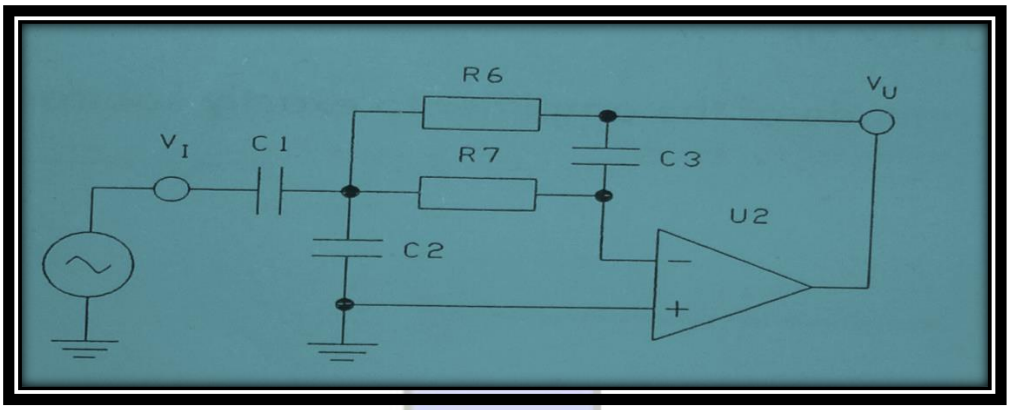


Figure 4-A: Setup of the experiment

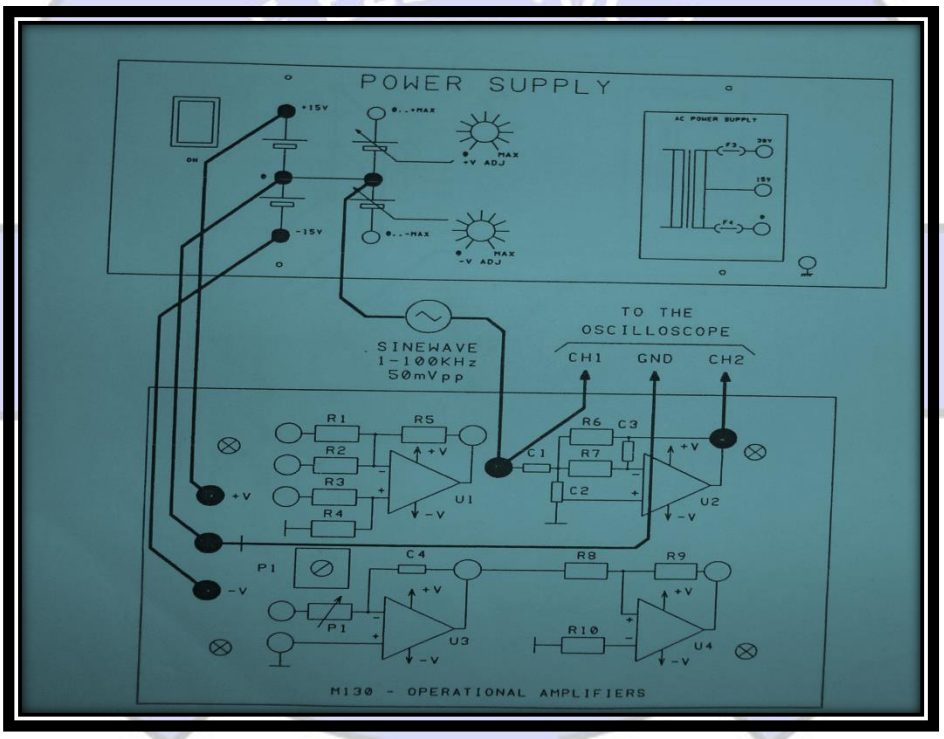


Figure 4-B: Practical wiring for the experiment

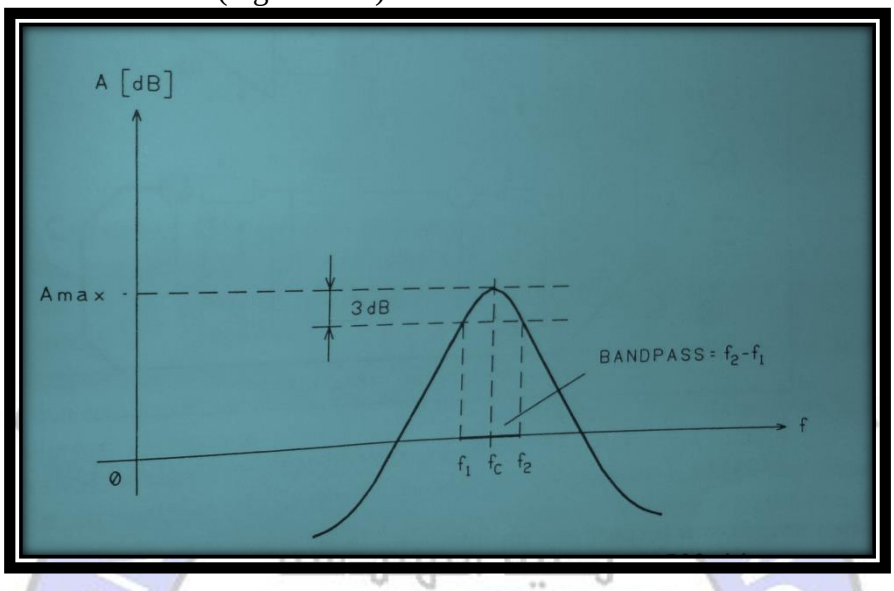
1- Apply a constant amplitude of sinewave input signal for example 50m Vpp and change the frequency in steps from 1KHz to 100 KHz. Note that the M130 is power supplied at +15 and -15.

2- The consequent output voltage is measured and recorded.

4- RESULTS:

1- Record the output voltage at step 2 from the procedures.

2- Plot the recorded output amplitudes in dB with the formula A= $20\log_{10}\frac{V_u}{V_i}$ on the vertical axis (linear) and the frequency on the horizontal axis (logarithmic)



5- Discussion:-

1- What are the advantages of active filters?

2- What are the applications of active filters?

3- List different designs of active band pass filters and specify their orders.

4- Can you predict the order of band pass active filter that was used in the lab?

University of Anbar
College of Engineering
Dept. of Electrical Engineering

Lab. Name: Electronic Lab./ 3rd Level
Experiment no.: 9
Lab. Supervisors: Mr. Hatem Al- Dulaimi,
Mss. Mariam R. Mirza,
Mr. Omar Al-Ani

Experimental Title: The triangle- square wave generator

1- OBJECTIVES:-

To implement triangle/ square wave generator.

2- INTRODUCTION AND THEORY:-

A sample triangle/ square wave generator made out of two OP AMP stages. The two stages are respectively an integrator and a comparator stages, whose operation is described as fallows(see figure 1):

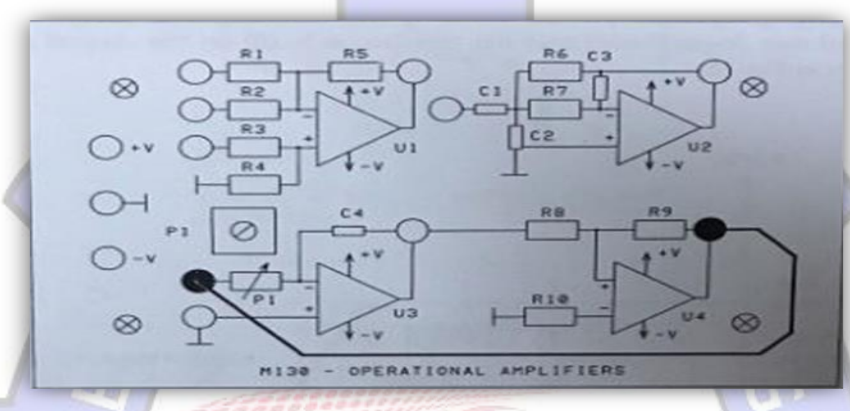


Figure 1:The triangle/ square wave generator

1- Integrator

In figure 2, Assume capacitor C is initially discharged. The voltage at the "-" terminal equals that of the output of the OP AMP and both equal 0. If a positive constant voltage is applied to R, current is following- in to charge the capacitor(we neglect the current into the "-" terminal).As the capacitor charges, the voltage of the " –" terminal tends to rise but this makes the amp output voltage to lower. This lowering of vo is fed- back to the "-" terminal by C and this ensures that the "-" terminal remains at ground voltage level. If this is so, resistor R continuous to lead- in a constant current, the capacitor charges linearly and the output voltage is a nice and clean straight line going towards saturation.

The slope of the output voltage waveform is dependent on the RC time constant, which in our sample circuit is adjustable, since R is a resistive trimmer.

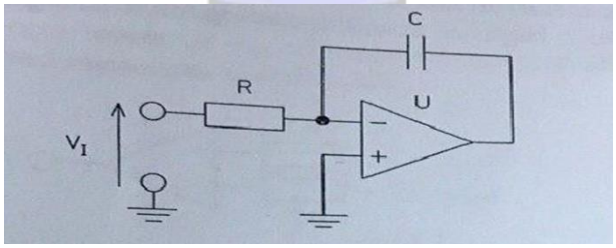


Figure 2:The Integrator

2- Comparator

A comparator is a device which matches the voltage of its " + " and "- " terminals and sets its output High or Low depending on the sign of the difference. See Figure 3.

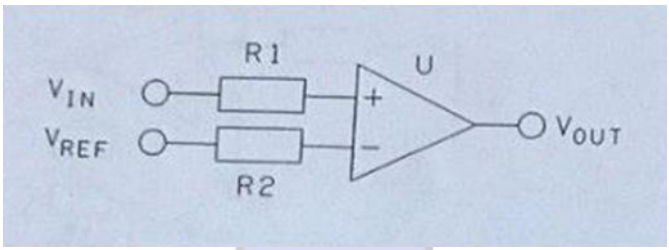


Figure 3: The votage comparator

An OP AMP can be used as a comparator by making it work in open loop, i.e. derived of its customary feedback resistor placed between its output and "-" input. In this manner the OP AMP amplifies the input voltage difference of a value of 1000 to 1 million times(typical open- loop gain of an op amp). Therefore the output rapidly swings from the " minus saturation" to the " plus saturation" status or vice- versa at each inversion of the sign of Vi(+) – Vi(-).

In order to introduce a Hysteresis effect,the comparator of the M130 is provided with positive feedback (Figure 4).

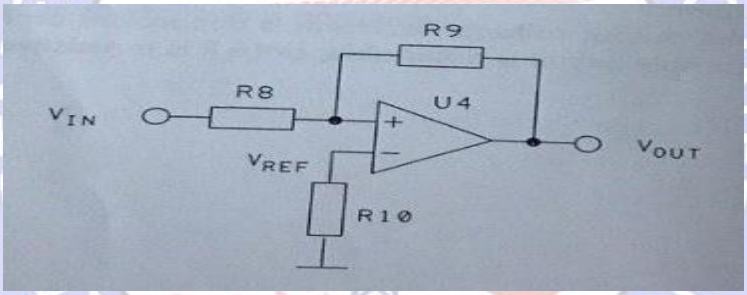


Figure 4: Comparator with hysteresis

Operation of the hysteresis mechanism is as follows:

Assume Vo is initially at the negative saturation voltage and Vin is made to rise. The actual voltage of the " + " terminal will be: $V(+)= Vin - \frac{Vin-Vo}{R1+R2} \times R1$

In other words, the negative Vo " pulls down" V(+) from the actual value of Vin. Vin will have to exceed Vref by a certain amount for he comparator to switch. The same holds when Vin is made to fall from a positive value. The Vref will have to be exceed for the comparator to switch back. The difference in voltage levels of Vin to make the comparator switch upwards and downwards is called Hysteresis (Figure 5).

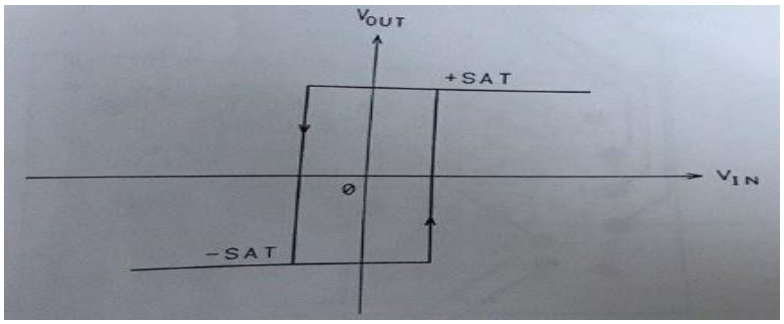


Figure 5: I/O characteristics of the comparator with hysteresis.

3- PROCEDURES and RESULTS:

In order to examine their operation of both the integrator and the comparator, set up the equipment as shown in figure 6, figure 7 shows same sample waveforms. Adjust the oscilloscope to make both traces appear on the screen.

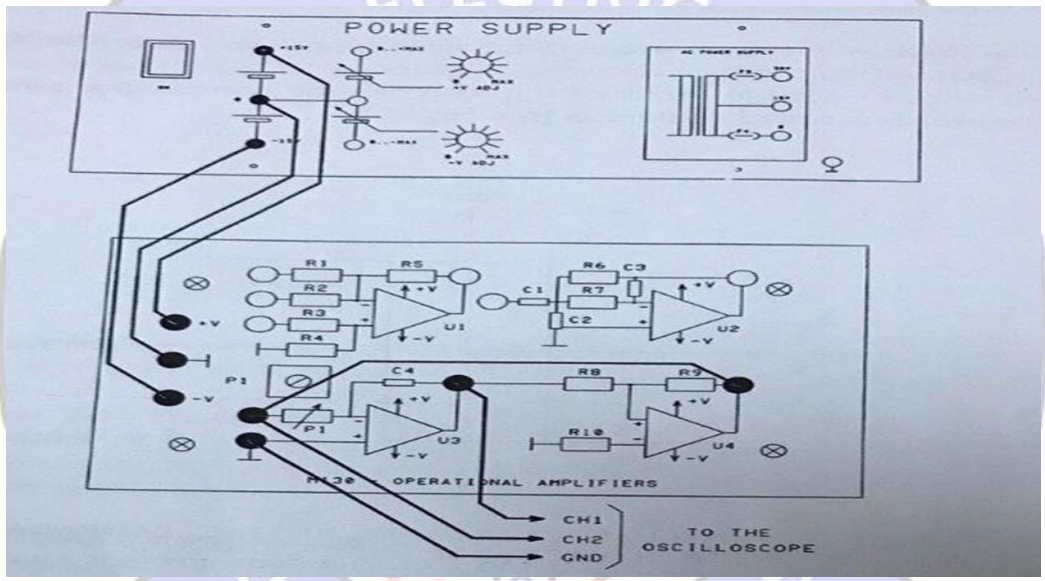


Figure 6: Setup for the study of the integrator and comparator in the waveform generator

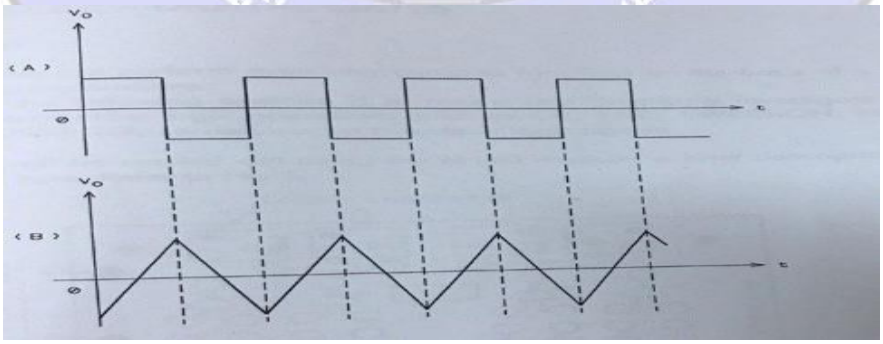
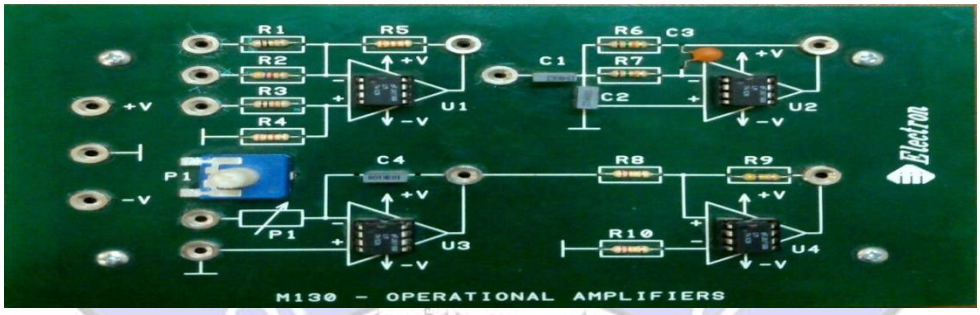


Figure 7: Waveshapes at the outputs of comparator (A) and Integrator (B)

From the image displayed at the scope measure and record:

- Period (and frequency) of the waves for various settings of P1. Measure P1 each time by removing power and the input cord to P1 and using an ohmmeter.
- Measure the peak- to- peak amplitude of the triangle wave and that of the square wave.
- Measure the hysteresis for the comparator.



5- Discussion:-

1-Discuss the operation of the hysteresis of the comparator.

2- What was the period of the triangle wave generator you observed experimentally? Using your actual circuit values, calculate the expected value for the period and compare it with the observed value.

University of Anbar
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Dept. of Electrical Engineering

Lab. Name: Electronic Lab./ 3rd Level
Experiment no.: 10
Lab. Supervisors: Mr. Hatem Al- Dulaimi,
Mss. Mariam R. Mirza,
Mr. Omar Al-Ani

Experimental Title Part-A: Voltage Regulator

1- OBJECTIVES:-

To implement voltage regulator circuit whenever the load is changed.

2- INTRODUCTION AND THEORY:-

Figure 1 shows the circuit under test. R6 is used as a load resistor.

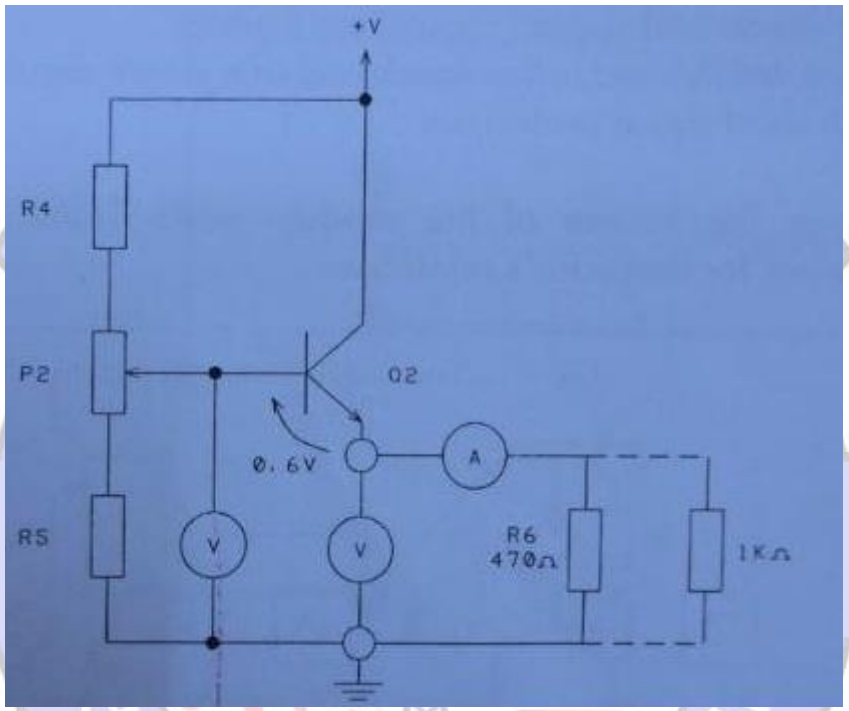
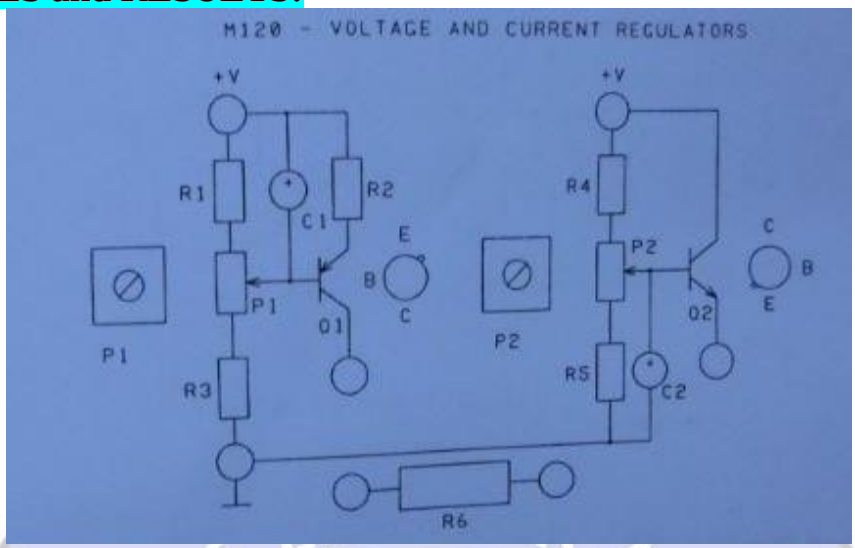


Figure 1: Circuit under study

The operation of the circuit is as follows:

Transistor Q2 appears wired as a Common Collector Amplifier. As long as Q2 is in the linear zone of its working characteristics, the Base-to- Emitter voltage is 0.6V (actually 0.5 t0 0.7V depending on the transistor type). Therefore, the Emitter- to- Ground voltage(voltage on the load) will equal the Base-to- Ground voltage less 0.6V. The Base to Ground voltage, which is determined by the setting of potentiometer P2. By moving P2 the load voltage can be adjusted as desired in a range limited by R4 and R5. These two resistors respectively prevent saturation (R4) and cut-off (R5) of transistor Q2. The stabilizing action of the circuit can be described as follows. Assume at a certain time the voltage on the load tends to drop: this drop in Emitter- to- Ground voltage can be reflect an equal change in Base- to – Ground voltage. More current will flow into the Base of Q2 and this will increse the emitter current, thus contrasting the initial changed assumed.

3- PROCEDURES and RESULTS:



Outline of the module M120

1- Record the output voltage of the regulator as the Base- to- Ground voltage is changed in steps of 1V each by means of P2.

2- Plot the results on a graph which should look like that of figure 2.

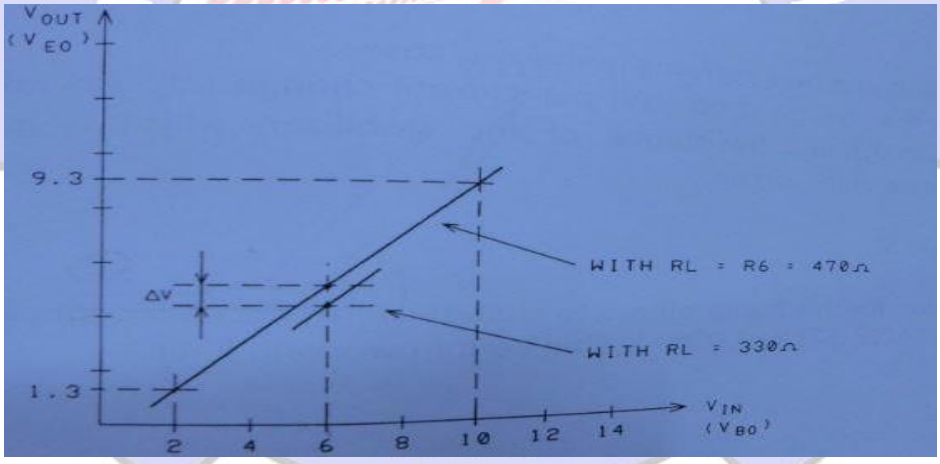


Figure 2: Sample results

3- Select a suitable working point, for instance for a 6V output voltage, and then impress a change in output current placing a 1K resistor in parallel to R6. Use the 1K, 2W resistor R1 of module M10.

4- Measure voltages and currents before placing the parallel resistor 1K Ω and after it.

5- Calculate the output dynamic resistance of the stabilizer. Rout= $\Delta V/\Delta I$

5- Discussion:-

1-Discuss the obtained value of Rout which is in an index of the performance of the circuit.

Experimental Title Part-B: Current Regulator

1- OBJECTIVES:-

To implement current regulator circuit whenever the load is changed.

2- INTRODUCTION AND THEORY:-

The circuit being studied is shown in figure

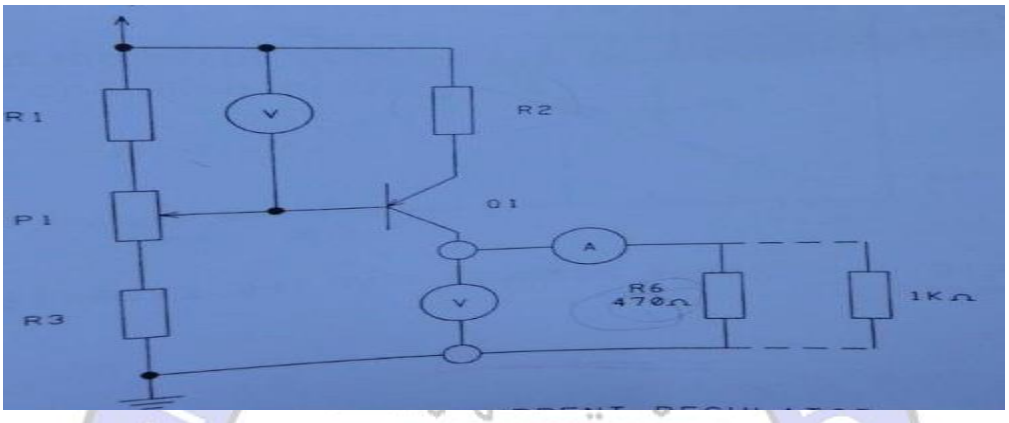


Figure 1: Circuit under study

It basically consists of a transistor amplifier in which the load is wired in the collector circuit.

P1 sets the bias point for Q1. The voltage on R2 is stabilized with the same mechanism as seen in the preceding experiment. Therefore also the current in R2 is stabilized and since the Emitter current of a transistor practically equals its collector current, also the load current is stabilized.

Double- check this by assuming that the load current changes (increases) for the same reason: The emitter current will also increase, as well as the voltage drops across it.

An increase of Emitter- to- Ground voltage will decrease the base current, since the base voltage bias is held constant by the input voltage divider. This will contrast the initial change assumed. Therefore, we have another negative feedback case, with its stabilizing effects.

3- PROCEDURES and RESULTS:

1- Record the input/ output characteristic of the circuit, record the output current of the regulator as the input voltage is changed in steps of 1V each by means of P1.

2- Plot the results on a graph which should look like that of the figure 2.

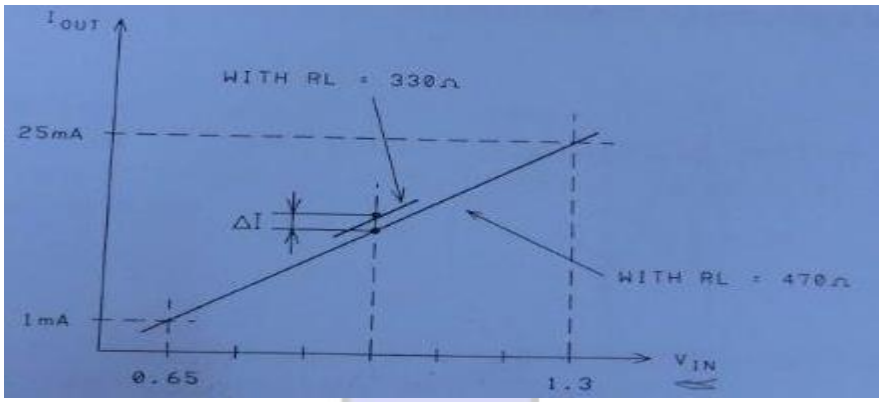


Figure 2: Sample results.

3- Select a suitable working point, for instance for a 6V output voltage, and then impress a change in output current placing a 1K resistor in parallel to R6. Use the 1K, 2W resistor R1 of module M10.

4- Measure voltages and currents before placing the parallel resistor 1K Ω and after it.

5- Calculate the output conductance of the stabilizer. Sout= $\Delta I/\Delta V$, Sout= 1/Rout

5- Discussion:-

1-Discuss the obtained value of Sout which is in an index of the performance of the circuit.

Experimental Title: Astable Circuit

1- OBJECTIVES:-

To implement astable circuit.

2- INTRODUCTION AND THEORY:-

The circuit under study is shown in figure 1.

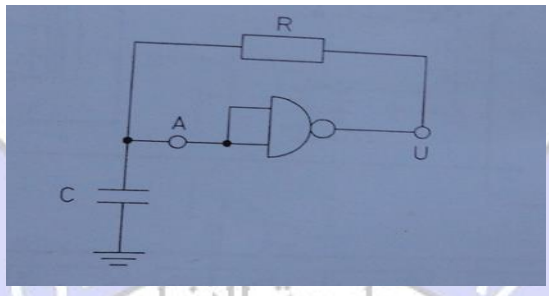


Figure 1:Circuit under study

Its operation is as follows:

- Assume C is initially discharged. It holds the gate- input low. The output is correspondingly high.
- Capacitor C charges through R and the voltage across it rises consequently, to the point where the gate switches its output and C starts discharging through R.
- The switching threshold of the gate is again met and the cycle is repeated. The light indicating the output level blinks. Typical waveshapes are shown in figure 2.

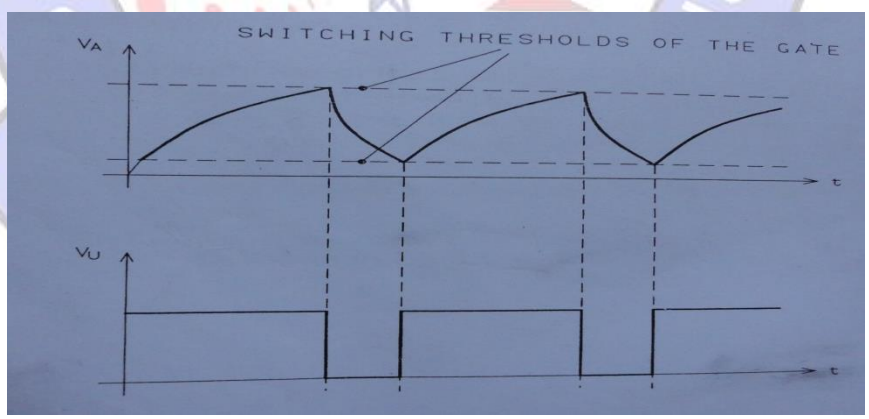


Figure 2: Waveshapes for the circuit of fig.1..

3- PROCEDURES and RESULTS:

The setup to study the astable operation is shown in figure 3.

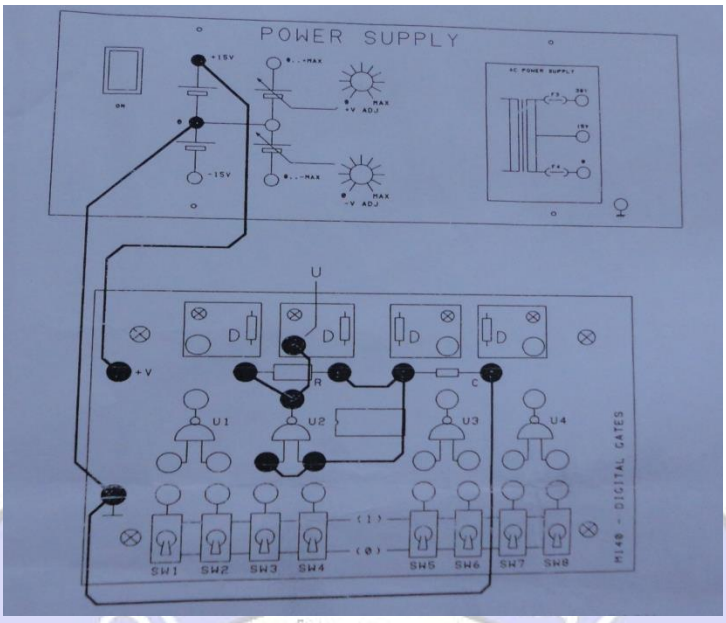


Figure 3: Setup to study the astable operation.

5- Discussion:-

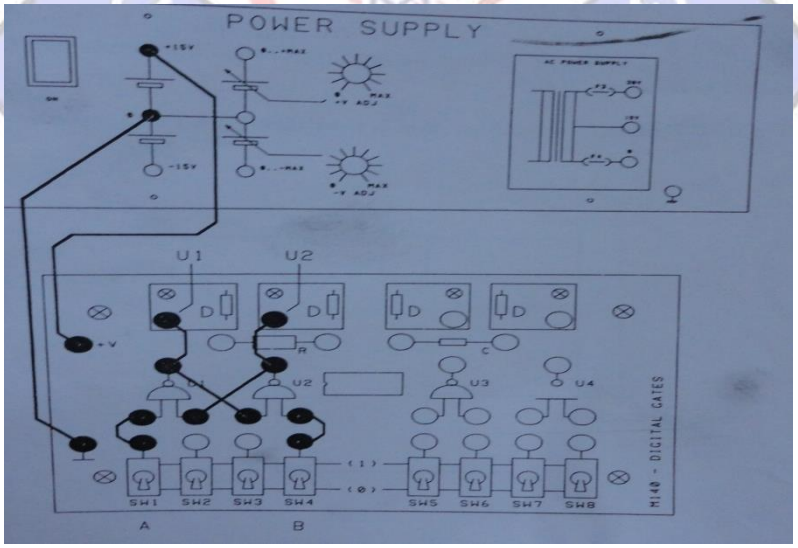
1- From your observations during the experiment, how you can define the astable behavior of the circuit

2- Find the duty cycle from the output waveform and compare it with its theoretical value.

3- Suggest another circuit which work as astable circuit.

Activity:

Regarding RS Bistable (Flip flop) and after complete its setup to study it using the figure below



Find its truth table after completing the connection of the circuit.

University of Anbar
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Dept. of Electrical Engineering

Lab. Name: Electronic Lab./ 3rd Level
Experiment no.: 12
Lab. Supervisors: Mr. Hatem Al- Dulaimi,
Mss. Mariam R. Mirza,
Mr. Omar Al-Ani

Experimental Title: Class A Power Amplifier

1- OBJECTIVES:- To calculate and measure DC and AC voltages and calculate the efficiency for class A power amplifier.

2- INTRODUCTION AND THEORY:-

There are classes of transistors according to the ratio of output signal to the input signal. These are A-AB-B-C classes. Operation classes of transistor are determined by base bias or in other words, work point on the load line. Operation bias of a transistor can be made by various methods. The most common methods are seen in figure 1

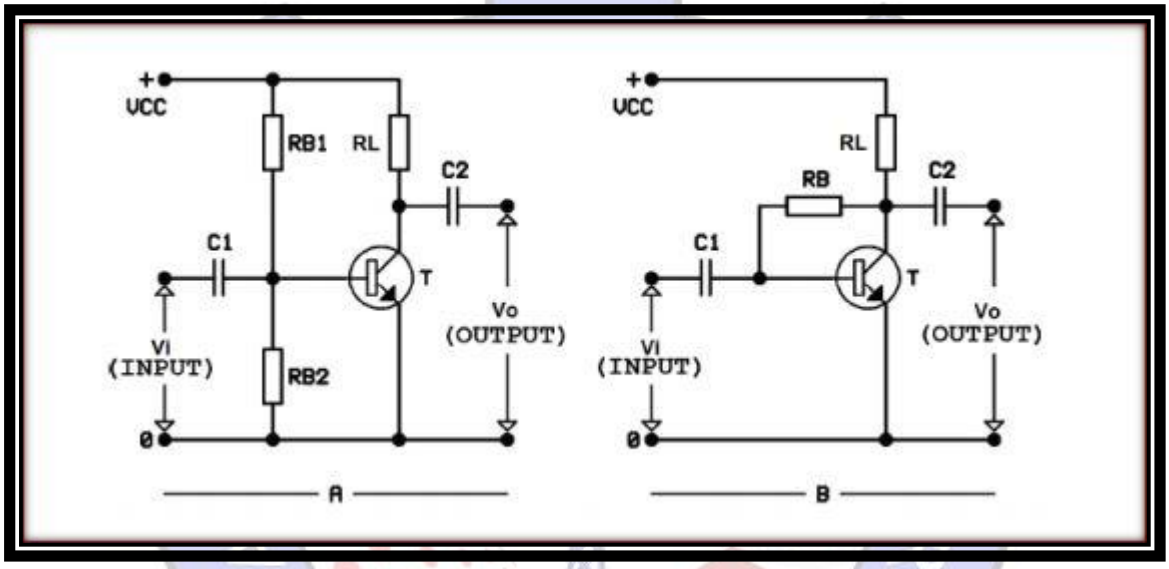

Figure 1: Emitter ground amplifier.

The transistor in figure 1 is an emitter ground amplifier. As we know it is the most common connection type. Operation classes of transistor are examined on this connection type in our experiment set. In figure 1.A, base bias is maintained by the RB1 and RB2 resistors from the supply voltage. This type of bias is called fixed bias. In figure 1.1B, base bias is sustained by collector voltage. During the work time of transistor, there is forward voltage from the supply and alternating voltage formed by the input signal. This voltage has a variable collector and this voltage controls the base in a negative direction because there is 180 of phase difference in emitter ground amplifiers. As you see, the base is negative charged from the collector and the gain is restricted. This type of bias is called "degenerative bias".

CLASS A AMPLIFIER:

The most important aspect of class A operation is that the output signal is not distorted. However, the productivity(Productivity of an amplifier is the supply energy it uses during the active work time.) is very low. Schema of a class A amplifier is shown in figure 2.

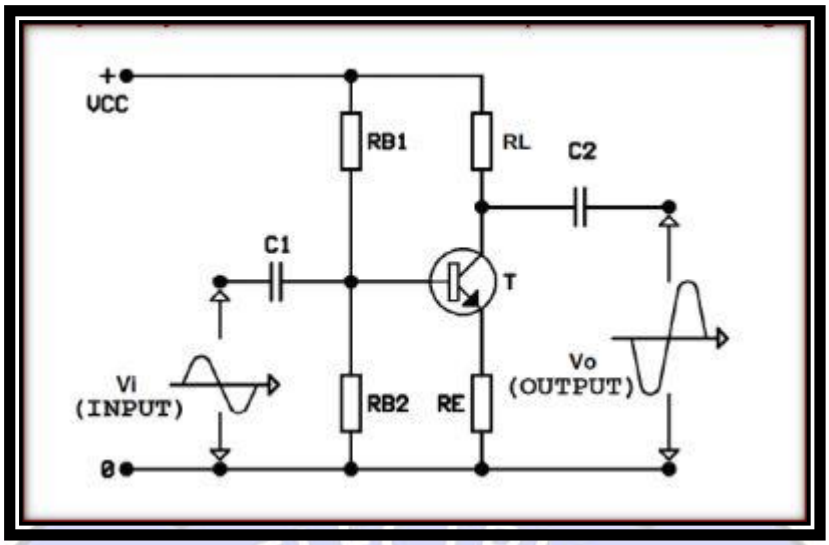

Figure 2: Class A amplifier.

In this type of amplifiers, load line and work point are determined by the graphics drawn by the help of Ic (collector current) and Vc (collector voltage). Current passes through collector even if there is no input signal. There is no distortion but the productivity is very low. Output and input signals are shown in figure3.

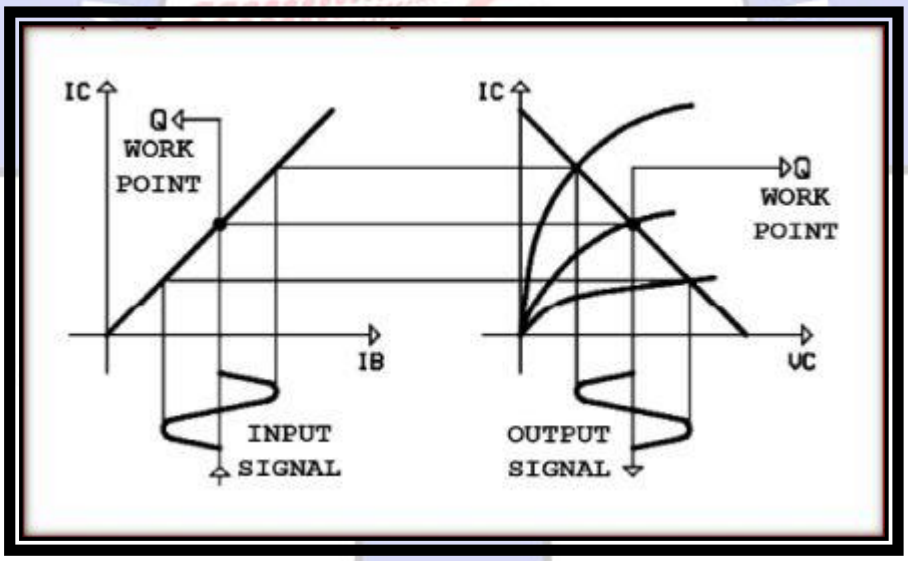

Figure 3: Output and input signals for class A amplifier.

A class- A amplifier draws the same power from the voltage supply regardless of the signal applied. The input power is calculated from:

$$P_i\,(\mathrm{DC}) = V_{CC} I_{DC} = V_{CC} I_{CQ}$$

The power provided by the amplifier can be calculated using:

$$P_o(\mathrm{AC}) = \frac{V_C^2(\mathrm{rms})}{R_C} = \frac{V_C^2(\mathrm{peak})}{2R_C} = \frac{V_C^2(\mathrm{p\text{-}p})}{8R_C}$$

With the amplifier's efficiency being:

$$\%\eta = 100 \times \frac{P_o\,(\mathrm{AC})}{P_i\,(\mathrm{DC})}\%$$

If the input is a sinusoidal, then the output is also sinusoidal over the DC biasing voltage(Figure 4).

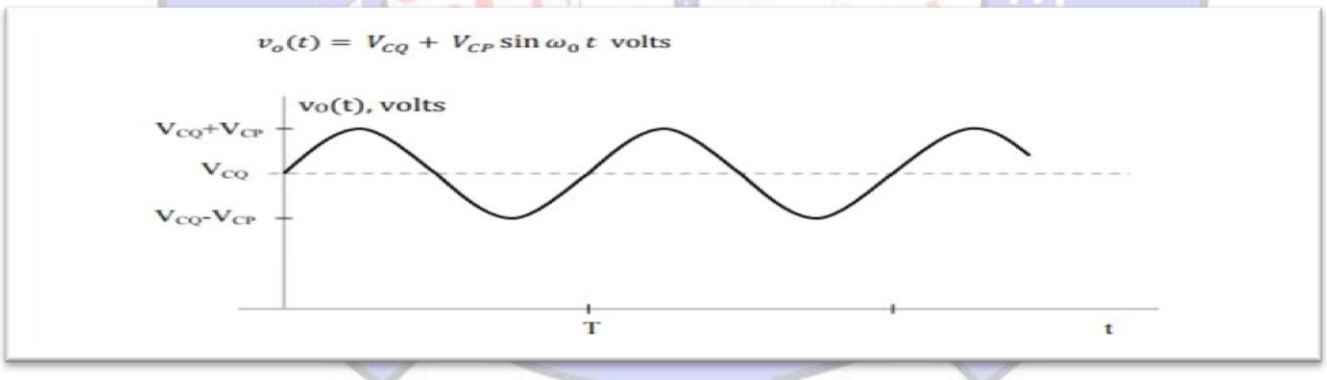

Figure 4

The useful AC power is then:

$$P_L = V_{CP}^2 / 2R_L$$

For the power delivered to the circuit, the power spent over the base circuitry is neglected and the average power delivered from the power supply is obtained as:

$$P_S = V_{CC}\, I_{CQ}$$

The power efficiency is defined as

$$\eta = P_L/P_S$$

or

$$\eta = V_{CP}^2/2V_{CC}\, I_{CQ}R_L$$

The maximum efficiency is reached if

$$V_{CQ} = V_{CC}/2 \text{ and } V_{CP} = V_{CC}/2 \text{ and } I_{CQ} = V_{CC}/2\, R_L$$

Under these conditions, the efficiency becomes:

$$\eta = 0.25 = 25\%$$

i.e.., the 25 percent of the power delivered to the circuit is obtained as useful load power.

3- PROCEDURES:

Part1: Class- A amplifier: DC bias.

a-Measure and record the DC bias values for the circuit in figure 5. Measure and record VB, VE, VC and IC.

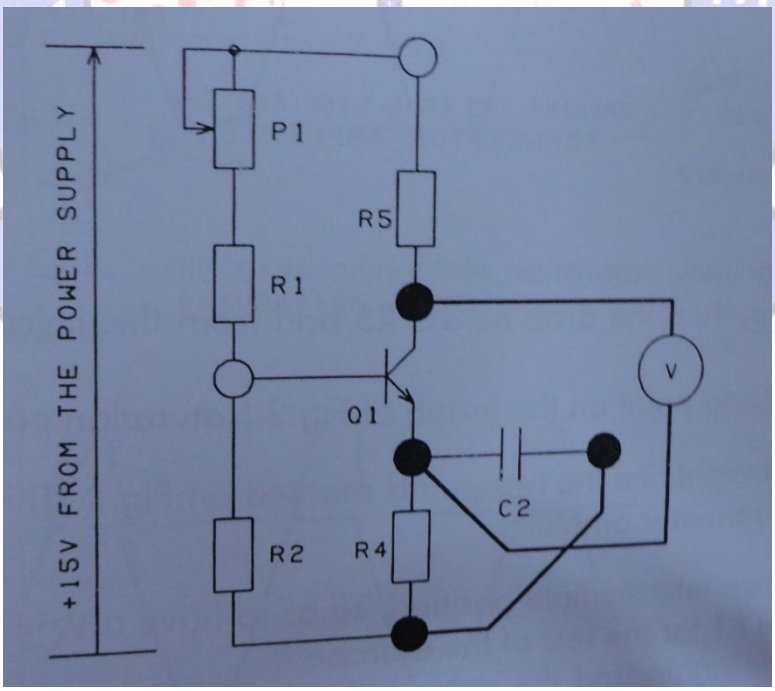

Figure 5: The DC biasing of class A amplifier.

Part 2: Class- amplifier: AC operation(figure 6).

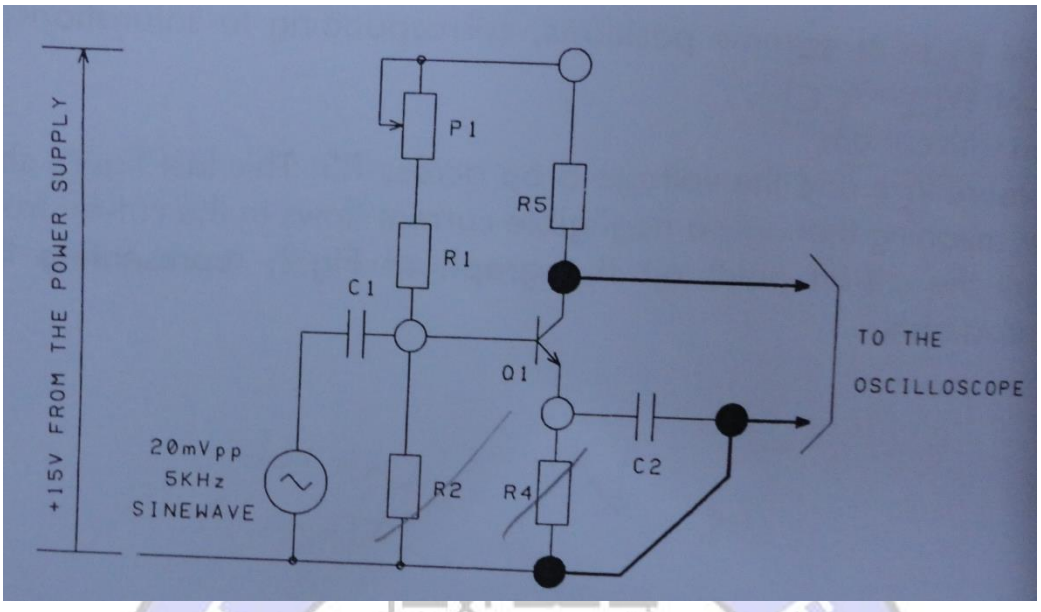

Figure 6: AC operation of class A amplifier.

a- Adjust the input signal to obtain the largest undistoreted output signal. Measure and record the input and output voltages.

b- Reduce the input signal to 0ne- half the level of step a. Measure and record the input and output voltages.

4- RESULTS:

1- Using the measured values in step a, calculate input power, output power and efficiency for class- A amplifier.
2- Using the measured values in step b, calculate input power, output power and efficiency for class- A amplifier

5- Discussion:-

1- Compare the calculated and measured values of power and efficiency obtained.

2- List different classes of amplifier and compare between them.